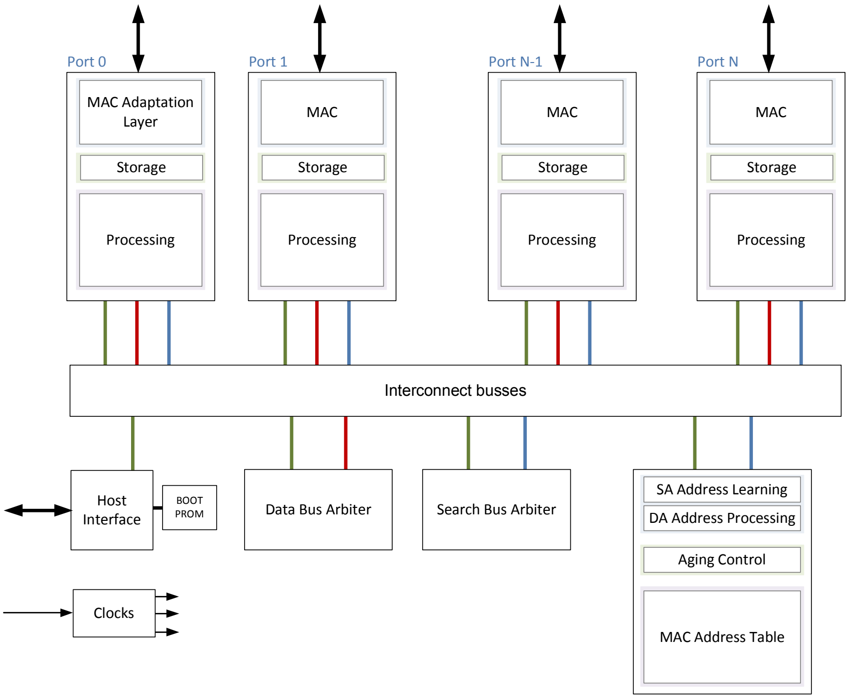
ESoCL

Ethernet Switch on Configurable Logic

Product Brief

Introduction



This document describes the Ethernet Switch on Configurable Logic, further referred to as ESoCL.

The ESoCL is a configurable Ethernet Switch that can be used to design Ethernet Switch functionality into FPGA based solutions to achieve a more flexible and integrated solution. The ESoCL supports up to 16 MAC ports, the MAC ports support an (R)MII or an (R)GMII MAC interface towards an external Ethernet PHY. Each MAC port has its own serial PHY management interface.

The ESoC is a VLAN capable Ethernet Switch. Untagged packets received by a port are tagged by the port default VLAN ID before they are processed. After switching an untagged packet to the destination port(s) the default tag is removed. Tagged packets can be re-tagged by the port default VLAN ID before or after they are processed further.

The ESoCL is a self-learning Ethernet Switch, the source address of incoming packets are stored or renewed in the internal MAC Address table, together with the associated VLAN ID. The MAC address table is monitored by an aging mechanism that removes expired MAC addresses.

The ESoCL can operate in unmanaged and managed mode. For unmanaged applications the ESoCL has an integrated boot ROM that can be used to configure the Ethernet Switch after reset is de- asserted. For managed applications the ESoCL has a generic, asynchronous, memory mapped interface that can be used by a processor platform to configure the Ethernet Switch. Managed applications with challenging start-up requirements related to the Ethernet Switch functionality can use the boot ROM as well.

Main Features

- Ethernet Switch with up to 16 ports
- Shared total switching capacity of 6-9 Gbps[1]
- Serial PHY management on each port
- Integrated Ethernet MACs with (R)MII or (R)GMII interface from Altera, Xilinx[2] or Open Cores[2].
- MAC address table with up to 8192 entries
- Configurable address learning and aging mechanism
- VLAN tagged frames, according to IEEE 802.1Q, up to 4096 VLAN ID's
- Generic host or Open Cores Wish Bone[3] interface
- Unmanaged and managed operation
- Initialization by boot ROM
- Extensive set of counters

Sources

- Synthesizable VHDL for FPGA targets[2]
- Semi-automated functional test bench

Target resources

Resources: 8 port ESoCL	Target: EP3CLS100F484I7 (Altera Cyclone 3LS)		
Units	**Logic cells**	**Memory bits**	**Fmax**
Generic (Arbiters, Control)	1217	8192 bits 1 M9K Block	CLK_CTRL ≤ 50MHz CLK_DATA ≤ 140MHz CLK_SEARCH ≤ 100MHz
RGMII Port (MAC, MAL, Storage, Processing)	5904	337328 bits 51 M9K Blocks	
Search engine	945	582400 bits 72 M9K Blocks	
Total	49394	337328 bits 481 M9K Blocks	

Documentation

- Product Brief
- Design Description
- Release Bulletin

[1] Depends on target device and average packet size

[2] Altera is supported, a Xilinx and a full Open Cores version are on the roadmap

[3] Open Cores Wish Bone interface is on the roadmap