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# **10\_100\_1000 Mbps Tri-mode Ethernet MAC Verification Plan**

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## Revision History

| Rev. | Date     | Author  | Description |
|------|----------|---------|-------------|
| 0.1  | 12/13/05 | Jon Gao | First Draft |
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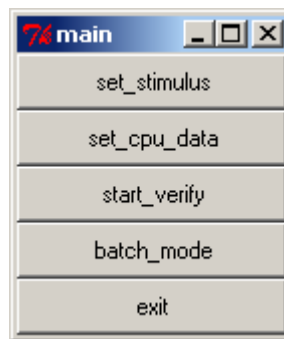
## 1

# TestCase List

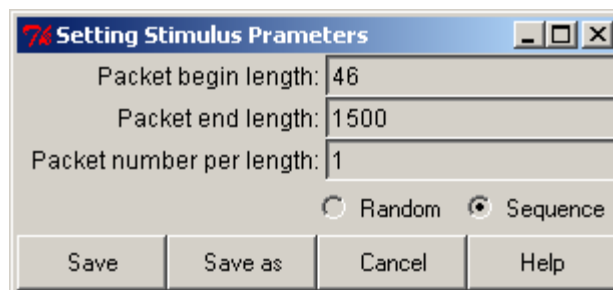
## 1.1 1000Mbps Full duplex 46-1500 length Packet throughout test

in the directory “rtl\_sim\ncsim\_sim\script” run script “run.tcl”

```
#vish run.tcl
```



select “set\_stimulus” to generate 46-1500 sequence packet .



select “start\_verify” at main frame. The script will call the ncsim simulation tools to verify the design. The packet sent to PHY will loop back to receiving port .When a “good” packet received , the following message will be printed:

the NO. 0001 IP Length is:0046 CRC-32check OK!

the NO. 0002 IP Length is:0047 CRC-32check OK!

the NO. 0003 IP Length is:0048 CRC-32check OK!

the NO. 0004 IP Length is:0049 CRC-32check OK!

the NO. ffff IP Length is:0050 CRC-32check OK!



### 1.2 100Mbps Full duplex 46-1500 length Packet throughput test

Press “set\_cpu\_data” button on main frame to set core to 100Mbps mode.

| RegName              | Address | default | Data   |
|----------------------|---------|---------|--------|
| Tx_Hwmark            | 0       | 0x001e  | 0x001e |
| Tx_Lwmark            | 1       | 0x0019  | 0x0019 |
| pause_frame_send_en  | 2       | 0x0000  | 0x0000 |
| pause_quanta_set     | 3       | 0x0000  | 0x0000 |
| IFGset               | 4       | 0x001e  | 0x001e |
| FullDuplex           | 5       | 0x0001  | 0x0001 |
| MaxRetry             | 6       | 0x0002  | 0x0002 |
| MAC_tx_add_en        | 7       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_data | 8       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_add  | 9       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_wr   | 10      | 0x0000  | 0x0000 |
| tx_pause_en          | 11      | 0x0000  | 0x0000 |
| xoff_cpu             | 12      | 0x0000  | 0x0000 |
| xon_cpu              | 13      | 0x0000  | 0x0000 |
| MAC_rx_add_chk_en    | 14      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_data | 15      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_add  | 16      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_wr   | 17      | 0x0000  | 0x0000 |
| broadcast_filter_en  | 18      | 0x0000  | 0x0000 |
| broadcast_MAX        | 19      | 0x0000  | 0x0000 |
| RX_APPEND_CRC        | 20      | 0x0000  | 0x0000 |
| Rx_Hwmark            | 21      | 0x001a  | 0x001a |
| Rx_Lwmark            | 22      | 0x0010  | 0x0010 |
| CRC_chk_en           | 23      | 0x0000  | 0x0000 |
| RX_IFG_SET           | 24      | 0x001e  | 0x001e |
| RX_MAX_LENGTH        | 25      | 0x2710  | 0x2710 |
| RX_MIN_LENGTH        | 26      | 0x0040  | 0x0040 |
| CPU_rd_addr          | 27      | 0x0000  | 0x0000 |
| CPU_rd_apply         | 28      | 0x0000  | 0x0000 |
| CPU_rd_grant         | 29      | 0x0000  | 0x0000 |
| CPU_rd_dout          | 30      | 0x0000  | 0x0000 |
| Line_loop_en         | 31      | 0x0000  | 0x0000 |
| Speed                | 32      | 0x0004  | 0x0002 |

Buttons: Save, SaveAs, Exit, Help

use the same way just like 1.1 to complete the simulation

### **1.3 10Mbps Full duplex 46-1500 length Packet throughout test**

refer to 1.2

### **1.4 Flow Control**

Setting Reg as folloing:

| RegName              | Address | default | Data   |
|----------------------|---------|---------|--------|
| Tx_Hwmark            | 0       | 0x001e  | 0x001e |
| Tx_Lwmark            | 1       | 0x0019  | 0x0019 |
| pause_frame_send_en  | 2       | 0x0000  | 0x0001 |
| pause_quanta_set     | 3       | 0x0000  | 0x000a |
| IFGset               | 4       | 0x001e  | 0x001e |
| FullDuplex           | 5       | 0x0001  | 0x0001 |
| MaxRetry             | 6       | 0x0002  | 0x0002 |
| MAC_tx_add_en        | 7       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_data | 8       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_add  | 9       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_wr   | 10      | 0x0000  | 0x0000 |
| tx_pause_en          | 11      | 0x0000  | 0x0001 |
| xoff_cpu             | 12      | 0x0000  | 0x0001 |
| xon_cpu              | 13      | 0x0000  | 0x0000 |
| MAC_rx_add_chk_en    | 14      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_data | 15      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_add  | 16      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_wr   | 17      | 0x0000  | 0x0000 |
| broadcast_filter_en  | 18      | 0x0000  | 0x0000 |
| broadcast_MAX        | 19      | 0x0000  | 0x0000 |
| RX_APPEND_CRC        | 20      | 0x0000  | 0x0000 |
| Rx_Hwmark            | 21      | 0x001a  | 0x001a |
| Rx_Lwmark            | 22      | 0x0010  | 0x0010 |
| CRC_chk_en           | 23      | 0x0000  | 0x0000 |
| RX_IFG_SET           | 24      | 0x001e  | 0x001e |
| RX_MAX_LENGTH        | 25      | 0x2710  | 0x2710 |
| RX_MIN_LENGTH        | 26      | 0x0040  | 0x0040 |
| CPU_rd_addr          | 27      | 0x0000  | 0x0000 |
| CPU_rd_apply         | 28      | 0x0000  | 0x0000 |
| CPU_rd_grant         | 29      | 0x0000  | 0x0000 |
| CPU_rd_dout          | 30      | 0x0000  | 0x0000 |
| Line_loop_en         | 31      | 0x0000  | 0x0000 |
| Speed                | 32      | 0x0004  | 0x0004 |

starting the verify, the simulation will output

Pause frame received :

Received Pause Quanta is :0x000a

At the same time, the transmit state machine will enter pause mode and delay packet send for 10 slot time.

### 1.5 Source MAC replace

edit CPU.dec as following:

```
12070001
12080030
120a0001
180a0000
18080031
18090001
180a0001
180a0000
18080032
18090002
180a0001
180a0000
18080033
18090003
180a0001
180a0000
18080034
18090004
180a0001
180a0000
18080035
18090005
180a0001
180a0000
```

received packet is:

```
0x000: 10 11 12 13 14 15 30 31 - 32 33 34 35 08 00 45 00
0x010: 00 2e 00 01 02 03 04 05 - 06 07 08 09 0a 0b 0c 0d
0x020: 0e 0f 10 11 12 13 14 15 - 16 17 18 19 1a 1b 1c 1d
```

0x030: 1e 1f 20 21 22 23 00 01 - 92 db e9 b7

The received packet source MAC address was replaced with “30 31 32 33 34 35”

## 1.6 Target MAC check

edit CPU.dec as following:

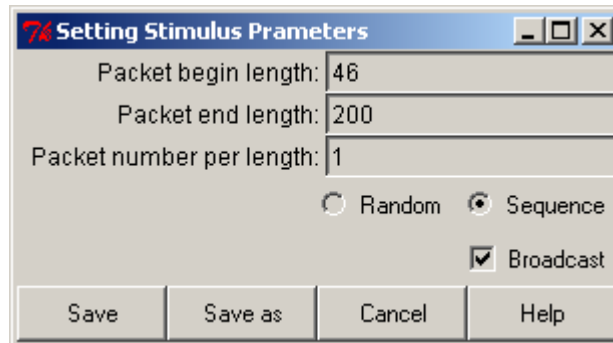
```
190e0001
190f0010
19100000
19110001
19110000
190f0011
19100001
19110001
19110000
190f0012
19100002
19110001
19110000
190f0013
19100003
19110001
19110000
190f0014
19100004
19110001
19110000
190f0015
19100005
19110001
19110000
```

all packets passed target MAC check and received ok.

When received packet can not pass the target MAC check , the packet will be dropped.

## 1.7 Broadcast filter test

Setting Stimulus as following windows:



Setting Reg config as following windows:

| RegName                   | Address | default | Data   |
|---------------------------|---------|---------|--------|
| Tx_Hwmark                 | 0       | 0x001e  | 0x001e |
| Tx_Lwmark                 | 1       | 0x0019  | 0x0019 |
| pause_frame_send_en       | 2       | 0x0000  | 0x0000 |
| pause_quanta_set          | 3       | 0x0000  | 0x0000 |
| IFGset                    | 4       | 0x001e  | 0x001e |
| FullDuplex                | 5       | 0x0001  | 0x0001 |
| MaxRetry                  | 6       | 0x0002  | 0x0002 |
| MAC_tx_add_en             | 7       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_data      | 8       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_add       | 9       | 0x0000  | 0x0000 |
| MAC_tx_add_prom_wr        | 10      | 0x0000  | 0x0000 |
| tx_pause_en               | 11      | 0x0000  | 0x0000 |
| xoff_cpu                  | 12      | 0x0000  | 0x0000 |
| xon_cpu                   | 13      | 0x0000  | 0x0000 |
| MAC_rx_add_chk_en         | 14      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_data      | 15      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_add       | 16      | 0x0000  | 0x0000 |
| MAC_rx_add_prom_wr        | 17      | 0x0000  | 0x0000 |
| broadcast_filter_en       | 18      | 0x0000  | 0x0001 |
| broadcast_bucket_depth    | 19      | 0x0000  | 0x0080 |
| broadcast_bucket_interval | 20      | 0x0000  | 0x0100 |
| RX_APPEND_CRC             | 21      | 0x0000  | 0x0000 |
| Rx_Hwmark                 | 22      | 0x001a  | 0x001a |
| Rx_Lwmark                 | 23      | 0x0010  | 0x0010 |
| CRC_chk_en                | 24      | 0x0000  | 0x0000 |
| RX_IFG_SET                | 25      | 0x001e  | 0x001e |
| RX_MAX_LENGTH             | 26      | 0x2710  | 0x2710 |
| RX_MIN_LENGTH             | 27      | 0x0040  | 0x0040 |
| CPU_rd_addr               | 28      | 0x0000  | 0x0000 |
| CPU_rd_apply              | 29      | 0x0000  | 0x0000 |
| Line_loop_en              | 32      | 0x0000  | 0x0000 |
| Speed                     | 33      | 0x0004  | 0x0004 |

The report of simulator look likes:

the NO. 0001 IP Length is:0046 CRC-32check OK!

the NO. 0006 IP Length is:0051 CRC-32check OK!

the NO. 0008 IP Length is:0053 CRC-32check OK!

the NO. 000d IP Length is:0058 CRC-32check OK!

the NO. 000f IP Length is:0060 CRC-32check OK!

the NO. 0011 IP Length is:0062 CRC-32check OK!

the NO. 0025 IP Length is:0082 CRC-32check OK!

the NO. 0027 IP Length is:0084 CRC-32check OK!

the NO. 002e IP Length is:0091 CRC-32check OK!

the NO. 0035 IP Length is:0098 CRC-32check OK!

the NO. 0038 IP Length is:0101 CRC-32check OK!

the NO. 003d IP Length is:0106 CRC-32check OK!

Some broadcast packets were dropped,because the broadcast flow exceed bandwidth limitation.