Ethernet IP Core

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Preliminary Draft

Revision History

Rev.	Date	Author	Description
0.1	13/03/01	Igor Mohor	First Draft
0.2	17/03/01	Igor Mohor	MDC clock divider changed. Instead of the clock select bits CLKS[2:0] the clock divider bits CLKDIV[7:0] are used.
1.0	21/03/01	Igor Mohor	MII module completed. Revision changed to 1.0 due to cvs demands.

Contents:

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Introduction

Ethernet IP Core consists of several modules (transmit, receive and control module making a MAC module, MII Management module and the Host Interface) and is capable of operating at 10 or 100 Mbit/s for Ethernet and Fast Ethernet applications. For the complete Ethernet solution an external PHY is needed.

2

IO ports

This section describes the Ethernet Core IO ports

2.1 Ethernet Core IO ports

Ethernet core is connected to the "world" by three types of signals:

- Host interface (connection to the RISC by the Wishbone)
- PHY Interface (connection to the PHY by the MII Management signals)
- Reset signals (for resetting different parts of the Ethernet core)

2.1.1 Host Interface ports

The below table contains the Ethernet IP Core to Host Interface ports. The host interface is WISHBONE Rev. B compliant.

WISHBONE COMPATIBLE

All signals listed below are active HIGH, unless otherwise noted. Signal direction is in respect to the Ethernet IP Core.

Port	Width	Direction	Description
CLK_I	1	I	Clock input
RST_I	1	I	Reset Input
ADDR_I	32	I	Address Input
DATA_I	32	I	Data Input
DATA_O	32	O	Data Output
SEL_I	4	I	Select Input Array Indicates which bytes are valid on data bus. Whenever this signal is not 1111b during a valid access, the ERR_O is asserted.
WE_I	1	I	Write Input

			Indicates a Write Cycle when asserted high or Read Cycle when asserted low.
STB_I	1	I	Strobe Input Indicates the beginning of a valid transfer cycle.
ACK_O	1	O	Acknowledgment Output Indicates a normal Cycle termination.
RTY_O	1	O	Retry Output Indicates that the interface is not ready, and the master should retry this operation.
DMA_REQ	1	O	DMA request
DMA_ACK	1	I	DMA acknowledgment
ERR_O	1	O	Error Acknowledgment Output Indicates an abnormal cycle termination.
INTA_O	1	O	Interrupt Output A.

Table 1: Host Interface Ports

2.1.2 PHY Interface ports

The below table contains the Ethernet IP Core to PHY Interface ports. All signals listed below are active HIGH, unless otherwise noted. Signal direction is in respect to the Ethernet IP Core.

Port	Width	Direction	Description
MTxClk	1	I	**Transmit Nibble or Symbol Clock**. The PHY provides the MTxClk signal. It operates at the frequency of 25 MHz (100 Mbit/s) or 2.5 MHz (10 Mbit/s). The clock is used as a timing reference for the transfer of MTxD[3:0], MTxEn and MTxErr.
MTxD[3:0]	4	O	**Transmit Data Nibble**. Signals are the transmit data nibble. They are synchronized to the rising edge of MTxClk. When MTxEn is asserted, PHY accepts the MTxD.
MTxEn	1	O	**Transmit Enable**. When asserted, signal indicates to the PHY that the data MTxD[3:0] is valid and the transmission can start. The transmission starts with the first nibble of the preamble. Signal remains asserted until all nibbles to be transmitted are presented to the PHY. It is deasserted prior to the first MTxClk following the final nibble of a frame.
MTxErr	1	O	**Transmit Coding Error**. When asserted for one MTxClk clock period while MTxEn is also asserted, it causes the PHY to transmit one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted to indicate that there has been a transmit coding error.

MRxClk	1	I	**Receive Nibble or Symbol Clock**. The PHY provides the MRxClk signal. It operates at the frequency of 25 MHz (100 Mbit/s) or 2.5 MHz (10 Mbit/s). The clock is used as a timing reference for the reception of MRxD[3:0], MRxDV and MRxErr.
MRxDV	1	I	**Receive Data Valid**. The PHY asserts this signal to indicate to the Rx MAC that it is presenting the valid nibbles on the MRxD[3:0] signals. Signal is asserted synchronously to the MRxClk. MRxDV is asserted from the first recovered nibble of the frame to the final recovered nibble. It is then deasserted prior to the first MRxClk that follows the final nibble.
MRxD [3:0]	4	I	**Receive Data Nibble**. Signals are the receive data nibble. They are synchronized to the rising edge of MRxClk. When MRxDV is asserted, the PHY sends a data nibble to the Rx MAC. For a correctly interpreted frame, seven bytes of a preamble and a completely formed SFD must be passed across the interface.
MRxErr	1	I	**Receive Error**. PHY asserts this signal to indicate to the Rx MAC that a media error was detected during the transmission of the current frame. MRxErr is synchronous to the MRxClk and is asserted for one or more MRxClk clock periods and then deasserted.
MColl	1	I	**Collision Detected**. The PHY asynchronously asserts the collision signal MColl after the collision is detected on the media. When deasserted, no collision is detected on the media.
MCRS	1	I	**Carrier Sense**. The PHY asynchronously asserts the carrier sense MCRS signal after the medium is detected in a non-idle state. When deasserted, signal indicates that the media is in the idle state (and the transmission can start).
MDC	1	O	**Management Data Clock**. Clock for the MDIO serial data channel.
MDIO	1	I/O	**Management Data Input/Output**. Bi-directional serial data channel for PHY/STA communication.

Table 2: PHY Interface Ports

2.1.3 Reset Signals

TBD. MAC sub-modules can be reset by one or more separate signals. To reset the PHY, we can use its RESET signal. The reset signal might be asserted by the boars system control register or by writing an appropriate bit in a PHY register that causes the PHY reset.

3

Registers

This section describes all base, control and status register inside the Ethernet IP Core. The Address field indicates a relative address in hexadecimal. Width specifies the number of bits in the register, and Access specifies the valid access types to that register. Where RW stands for read and write access, RO for read only access. A 'C' appended to RW or RO, indicates that some or all of the bits are cleared after a read.

Name	Address	Width	Access	Description
MODER	0x00	32	RW	Mode Register
INT_SOURCE	0x01	32	RW	Interrupt Source Register
INT_MASK	0x02	32	RW	Interrupt Mask Register
IPGT	0x03	32	RW	Back to Back Inter Packet Gap Register
IPGR1	0x04	32	RW	Non Back to Back Inter Packet Gap Register 1
IPGR2	0x05	32	RW	Non Back to Back Inter Packet Gap Register 2
PACKETLEN	0x06	32	RW	Packet Length (minimum and maximum) register
COLLCONF	0x07	32	RW	Collision and Retry Configuration
TX_BD_BASE_ADDR	0x08	32	RW	Transmit Buffer Descriptor Base Address Reg. First transmit buffer descriptor is located at the TX_BD_BASE_ADDR.
RX_BD_BASE_ADDR	0x09	32	RW	Receive Buffer Descriptor Base Address Reg. First receive buffer descriptor is located at the RX_BD_BASE_ADDR.
CTRLMODER	0x0A	32	RW	Control Module Mode Register
MIIMODER	0x0B	32	RW	MII Mode Register
MIICOMMAND	0x0C	32	RW	MII Commend Register
MIIADDRESS	0x0D	32	RW	MII Address Register Contains the PHY address and the register within the PHY address.
MIITX_DATA	0x0E	32	RW	MII Transmit Data The data to be transmitted to the PHY.
MIIRX_DATA	0x0F	32	RW	MII Receive Data The data received from the PHY.
MIISTATUS	0x10	32	RW	MII Status Register
MAC_ADDR0	0x11	32	RW	MAC Individual Address0 The LSB four bytes of the individual address are written to this register.

MAC_ADDR1	0x12	32	RW	MAC Individual Address1 The MSB two bytes of the individual address are written to this register.

Table 3: Register List

3.1 MODER (Mode Register)

Bit #	Access	Description
31-20		Reserved
19	RW	TXEN – Transmit Enable 0 = Transmit is disables 1 = Transmit is enabled
18	RW	RXEN – Receive Enable 0 = Receive is disables 1 = Receive is enabled
17	RW	RECSMALL - Receive Small Packets 0 = Packets smaller than MINFL are ignored. 1 = Packets smaller than MINFL are accepted.
16	RW	PASSALL – Pass All Receive Frames 0 = Control frames are not passed to the host. MAC Control module is enabled. 1 = All received frames are passed to the host. MAC Control module is disabled.
15	RW	PAD – Padding enabled 0 = Do not add pads to short frames 1 = Add pads to short frames (until the minimum frame length is equal to MINFL).
14	RW	HUGEN – Huge Packets Enable 0 = The maximum frame length is MAXFL. Bytes after that are discarded. 1 = Frames up to 32 kB are transmitted.
13	RW	CRCEN – CRC Enable 0 = Tx MAC does not append the CRC (passed frames already contain the CRC. 1 = Tx MAC appends the CRC to every frame.
12	RW	DLYCRCEN – Delayed CRC Enabled 0 = Normal operation (CRC calculation starts immediately after the SFD). 1 = CRC calculation starts 4 bytes after the SFD.
11	RW	RST – Reset MAC (do we need/want to reset the modules separately?)

		0 = Normal operation. 1 = MAC is reset.
10	RW	FULLD – Full Duplex 0 = Half duplex mode. 1 = Full duplex mode.
9	RW	EXDFREN – Excess Defer Enabled 0 = When the excessive deferral limit reached a packet is aborted. 1 = MAC waits for the carrier indefinitely.
8	RW	NOBCKOF – No Backoff 0 = Normal operation (a binary exponential backoff algorithm is used). 1 = Tx MAC starts retransmitting immediately after the collision.
7	RW	BCKPRESS – Back Pressure 0 = Normal operation 1 = Back pressure active. Signal FLSCRS is activated.
6	RW	BCKPNBEN – Back Pressure No Backoff Enabled 0 = Backoff enabled when in back pressure mode. 1 = Backoff disabled when in back pressure mode (transmission starts immediately after the collision).
5	RW	PRO – Promiscuous 0 = Check the destination address of the incoming frames. 1 = Receive the frame regardless of its address.
4	RW	IAM – Individual Address Mode 0 = Normal operation (Physical address is checked when the frame is received. 1 = The individual hash table is used to check all individual addresses that are received.
3	RW	BRO – Broadcast Address 0 = Receive all frames containing the broadcast address 1 = Reject all frames containing the broadcast address unless the PRO bit = 1.
2	RW	NOPRE – No Preamble 0 = Normal operation (7-byte preamble) 1 = No preamble is send
1	RW	ENTX – Enable Transmit 0 = Transmit disabled 1 = Transmit Enabled
0	RW	ENRX – Enable Receive 0 = Receive disabled 1 = Receive Enabled

Table 4: MODER Register

Reset Value:

MODER: 0000A000h

3.2 INT_SOURCE (Interrupt Source Register)

Bit #	Access	Description
31-5		Reserved
4	RW	BUSY - Busy Bit indicates that a buffer was received and discarded due to a lack of buffers.
3	RW	RXF - Receive Frame Bit indicates that a complete frame was received.
2	RW	RXB - Receive Buffer Bit indicates that a buffer was received (not a complete frame).
1	RW	TXE - Transmit Error Bit indicates that a buffer was not transmitted due to a transmit error.
0	RW	TXB - Transmit Buffer Bit indicates that a buffer has been transmitted.

Table 5: INT_SOURCE Register

Reset Value:

INT_SOURCE: 00000000h

3.3 INT_MASK (Interrupt Mask Register)

Bit #	Access	Description
31-5		Reserved
4	RW	BUSY_M - Busy Mask 0 = Event masked. 1 = Event causes an interrupt.
3	RW	RXF_M - Receive Frame Mask 0 = Event masked. 1 = Event causes an interrupt.
2	RW	RXB_M - Receive Buffer Mask 0 = Event masked. 1 = Event causes an interrupt.
1	RW	TXE_M - Transmit Error Mask 0 = Event masked. 1 = Event causes an interrupt.
0	RW	TXB_M - Transmit Buffer Mask 0 = Event masked.

		1 = Event causes an interrupt.

Table 6: INT_MASK Register

Reset Value:
INT_MASK: 00000000h

3.4 IPGT (Back to Back Inter Packet Gap Register)

Bit #	Access	Description
31-7		Reserved
6-0	RW	IPGT - Back to Back Inter Packet Gap Full Duplex: The recommended value is 0x15, which equals to 0.96 µs IPG (100 Mbit/s) or 9.6 µs (10 Mbit/s). The desired period in nibble times minus 6 should be written to the register. Half Duplex: The recommended value and default is 0x12, which equals to 0.96 µs IPG (100 Mbit/s) or 9.6 µs (10 Mbit/s). The desired period in nibble times minus 3 should be written to the register.

Table 7: IPGT Register

Reset Value:
IPGT: 00000012h

3.5 IPGR1 (Non Back to Back Inter Packet Gap Register 1)

Bit #	Access	Description
31-7		Reserved
6-0	RW	IPGR1 - Non Back to Back Inter Packet Gap 1 When carrier sense appears within the IPGR1 window, Tx MAC defers and the IPGR counter is reset. When carrier sense appears later then the IPGR1 window, the IPGR counter continuous counting. The recommended and default value for this register is 0xC and must be within the range [0,IPGR2].

Table 8: IPGR1 Register

Reset Value:
IPGR1: 0000000Ch

3.6 IPGR2 (Non Back to Back Inter Packet Gap Register 2)

Bit #	Access	Description
31-7		Reserved
6-0	RW	IPGR2 - Non Back to Back Inter Packet Gap 2 The recommended and default value is 0x12, which equals to 0.96 µs IPG (100 Mbit/s) or 9.6 µs (10 Mbit/s).

Table 9: IPGR2 Register

Reset Value:
IPGR2: 00000012h

3.7 PACKETLEN (Packet Length Register)

Bit #	Access	Description
31-16	RW	MINFL - Minimum Frame Length Minimum Ethernet packet is 60 bytes long. If a reception of smaller frames is needed, assert the RECSMALL bit (in the mode register MODER) or change the value of this register. To transmit small packets, assert the PAD bit or the MINFL value. (See the PAD bit description in the MODER register).
15-0	RW	MAXFL - Maximum Frame Length Maximum Ethernet packet is 1518 bytes long. To support this and to leave some additional space for the tags, a default maximum packet length equals to 1536 bytes (0x0600). If there is a need to support bigger packets, you can assert the HUGEN bit or increase the value of the MAXFL field. (See the HUGEN bit description in the MODER).

Table 10: PACKETLEN Register

Reset Value:
PACKETLEN: 003C0600h

3.8 COLLCONF (Collision and Retry Configuration Register)

Bit #	Access	Description
31-16	RW	MAXRET - Maximum Retry This field specifies the maximum number of consequential retransmission attempts after the collision is detected. When the maximum number is reached the Tx MAC reports an error and stops transmitting the current packet. According to the Ethernet standard, the MAXRET default value is set to 0xf (15).
15-0	RW	COLLVALID - Collision Valid This field specifies a collision time window. Collision that occurs later than the time window is reported as a »Late Collisions« and transmission of the current packet is aborted. The default value equals to 0x40 (64 bytes from the preamble).

Table 11: COLLCONF Register

Reset Value:

COLLCONF: 000F0040h

3.9 TX_BD_BASE_ADDR (Transmit BD Base Address Reg.)

Bit #	Access	Description
31:0	RW	Transmit Buffer Descriptor Base address Pointer to the first Tx BD (Transmit Buffer Descriptor)

Table 12: TX_BD_BASE_ADDR Register

Reset Value:

TX_BD_BASE_ADDR: 00000000h

3.10 RX_BD_BASE_ADDR (Receive BD Base Address Reg.)

Bit #	Access	Description
31:0	RW	Receive Buffer Descriptor Base address Pointer to the first Rx BD (Receive Buffer Descriptor)

Table 13: RX_BD_BASE_ADDR Register

Reset Value:

RX_BD_BASE_ADDR: 00000000h

3.11 CTRLMODER (Control Module Mode Register)

Bit #	Access	Description
31-16	RW	TPTV – Transmit PAUSE Timer Value
15-4		Reserved
3	RW	TXFLOW – Transmit Flow Control 0 = PAUSE control frames are blocked. 1 = PAUSE control frames are allowed to be send.
2	RW	RXFLOW – Receive Flow Control 0 = Received PAUSE control frames are ignored. 1 = Transmit function (Tx MAC) is blocked when a PAUSE control frame is received.
1	RW	PASSALL 0 = Pass only data packets to the upper layer (control frames are not passed). 1 = All packets are passed.
0	RW	TPRQ 0 = No transmit is requested. 1 = Transmit PAUSE control frame is requested.

Table 14: CTRLMODER Register

Reset Value:

CTRLMODER: 00000000h

3.12 MIIMODER (MII Mode Register)

Bit #	Access	Description
31-10		Reserved
9	RW	SCANINCR – Scan Increment 0 = The read of the status register in the same PHY will be performed all the time. 1 = The FIAD[4:0] will be incremented on every read. Starting address is 1, ending address is written in the FIAD[4:0].

8	RW	MIINOPRE – No Preamble 0 = 32-bit preamble send 1 = no preamble send
7-0	RW	CLKDIV – Clock Divider The field is a host clock divider factor. The host clock can be divided by an even number, greater then 1. The default value is 0x64 (100).

Table 15: MIIMODER Register

Reset Value:

MIIMODER: 00000064h

3.13 MIICOMMAND (MII Command Register)

Bit #	Access	Description
31-3		Reserved
2	RW	WCTRLDATA – Write Control Data
1	RW	RSTAT – Read Status
0	RW	SCANSTAT – Scan Status

Table 16: MIICOMMAND Register

Reset Value:

MIICOMMAND: 00000000h

3.14 MIIADDRESS (MII Address Register)

Bit #	Access	Description
31-13		Reserved
12-8	RW	RGAD – Register Address (within the PHY selected by the FIAD[4:0])
7-5		Reserved
4-0	RW	FIAD – PHY Address

Table 17: MIIADDRESS Register

Reset Value:

MIIADDRESS: 00000000h

3.15 MIITX_DATA (MII Transmit Data)

Bit #	Access	Description
31-16		Reserved
15-0	RW	CTRLDATA – Control Data (data to be written to the PHY)

Table 18: MIITX_DATA Register

Reset Value:
MIITX_DATA: 00000000h

3.16 MIIRX_DATA (MII Receive Data)

Bit #	Access	Description
31-16		Reserved
15-0	RW	PRSD – Received Data (data read from the PHY)

Table 19: MIIRX_DATA Register

Reset Value:
MIIRX_DATA: 00000000h

3.17 MIISTATUS (MII Status Register)

Bit #	Access	Description
31-11		Reserved
10	R	SCAN – Scan Operation in progress 0 = No scan operation in progress. 1 = Scan operation in progress.
9	R	NVALID – Invalid 0 = The data in the MSTATUS register is valid. 1 = The data in the MSTATUS register is invalid.
8	R	BUSY 0 = The MII is ready. 1 = The MII is busy (operation in progress).

7-3		Reserved
2	R	SPEED 0 = 10 Mb/s speed 1 = 100 Mb/s speed
1	R	DUPLEX 0 = Half duplex 1 = Full duplex
0	R	LINKOK: 0 = Fail 1 = Link OK

Table 20: MIISTATUS Register

Reset Value:

MIISTATUS: 00000000h

3.17 MAC_ADDR0 (MAC Address Register 0)

Bit #	Access	Description
31-16	RW	Bytes 3 and 2 of the Ethernet MAC address (individual address)
15-0	RW	Bytes 1 and 0 of the Ethernet MAC address (individual address)

Table 21: MAC_ADDR0 Register

Reset Value:

MAC_ADDR0: 00000000h

3.18 MAC_ADDR1 (MAC Address Register 1)

Bit #	Access	Description
31-16		
15-0	RW	Bytes 6 and 5 of the Ethernet MAC address (individual address)

Table 22: MAC_ADDR1 Register

Reset Value:

MAC_ADDR1: 00000000h

4 Operation

This section describes the Ethernet IP Core operation.

The core consists of four modules:

- Host interface connects the host to the rest of the system via the Wishbone. It also takes care for the transmit and receive buffer descriptors (BD).
- TX Ethernet MAC performs transmit function.
- RX Ethernet MAC performs receive function.
- MAC Control Module performs flow control function.
- MII Management Module performs PHY control and gathers the status information from it.

All modules together perform a full function 10/100 Mbit/s Media Access Control. The Ethernet core can operate in a half or a full duplex mode. The basic of the Ethernet is CSMA/CD protocol. The CSMA/CD stands for Carrier Sense Multiple Access / Collision Detection.

In half duplex mode when a station wants to transmit, it has to observe the activity on the media (Carrier Sense). As soon as the media is idle (no one is transmitting), any station can start with the transmission (Multiple Access). If two or more stations are transmitting at the same time, a collision on the media is detected. All stations stop transmitting and back-off for some random time. After the back-off time, the station checks the activity on the media again. If the media is idle, it starts transmitting. All other stations wait for the current transmission to end.

In full duplex mode the carrier sense and the collision detect signals are ignored. Flow control is achieved by sending and receiving the PAUSE control frames (see the TXFLOW and RXFLOW bit description in the MODER register). The MAC Control module takes care of that.

MII Management module provides a media independent interface (MII) to the external PHY. Using MIIM module a PHY configuration and status registers can be read/write.

4.1 Host Interface Operation and BD configuration

The host interface connects the Ethernet IP core to the rest of the system (RISC, memory) via the Wishbone bus. The Wishbone is used for accessing the configuration registers, buffer descriptors (BD) and the memory.

The function of the configuration registers is transparent and can be easily understood by reading the Registers section (Section 3) on the page X.

The transmission and the reception processes are based on the buffer descriptors (BD). The transmit buffer descriptors (TxBD) are used for transmitting the packets while the receive buffer descriptors (RxBD) are used for receiving them. Both are saved in the external memory at the address that is written in the TX_BD_BASE_ADDR and RX_BD_BASE_ADDR registers. The BDs are 8 bytes long and contain the status and length information of the packet to be send, together with the pointer that points to the packet saved in the external memory.

When the host wants to transmit the first packet, it has to write the packet to the external memory and set the first transmit BD (TxBD is located at the TX_BD_BASE_ADDR address) to point to that memory. Besides the pointer the packet length has to be set and the status cleared. When the packet and the BD are ready, a READY bit in the BD can be asserted. The host interface constantly copies the pointed BD to its internal BD buffer via the Wishbone and then checks its ready bit. Once the ready bit is asserted, it reads the first four bytes of the packets (from the address saved in the BD) to its internal packet buffer and sets the signals to notify the Tx MAC to start the transmission. While the transmission of this four bytes is in progress, it increments the BD pointer to point to the next four bytes and decrements the length by four bytes. Once the whole packet is send (length <= 0), the status field within the BD is updated. Then the pointer to the BDs is incremented and points to the next BD (TX_BD_BASE_ADDR + 1). The cycle repeats and the BD pointer is incremented by one each time. When a BD with the WRAP bit asserted is found, the BD pointer is not incremented but points again to the first BD (at the TX_BD_BASE_ADDR). A simplified BD logic is shown on the Figure 1: Tx BD Logic.

When the host receives the first packet, the packet is written to the external memory via the Wishbone. The packets address within the memory is written to the first receive BD (RxBD is located at the RX_BD_BASE_ADDR). When a packet or a whole frame is received an interrupt is generated, informing the host about the packet received.
The BD pointer is incremented by one.

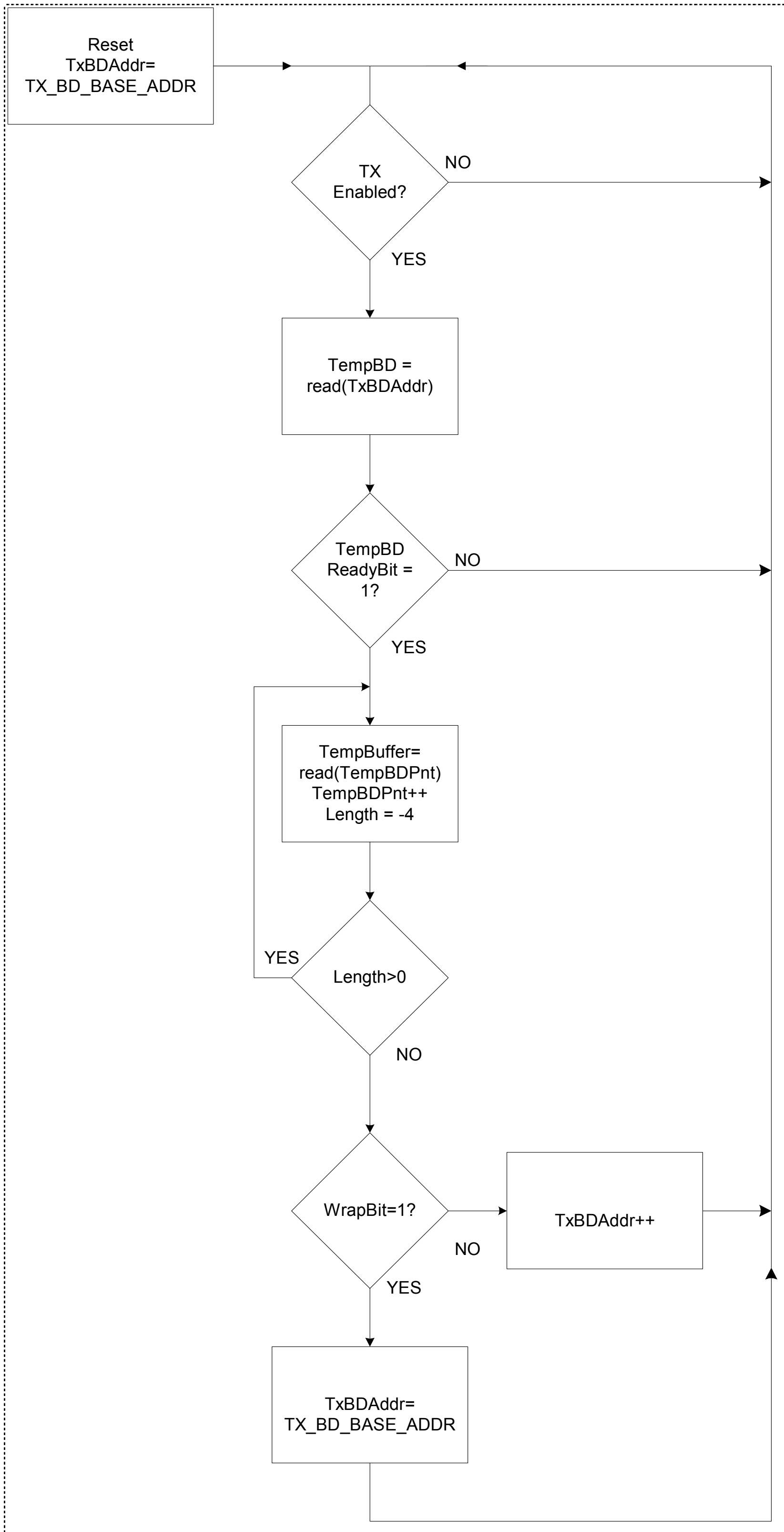


Figure 1: Tx BD Logic

4.2 TX Ethernet MAC

TX Ethernet MAC generates 10BASE-T/100BASE-TX transmit MII nibble data streams in response to the byte streams supplied from the transmit logic (host). It performs the required deferral and Backoff algorithms, takes care of the inter packet gap (IPG), computes the checksum (FCS) and monitors the physical media (by monitoring Carrier Sense and collision signals).

4.3 RX Ethernet MAC

RX Ethernet MAC transmits the data streams in response to the 10BASE-T or 100BASE-TX receive MII nibbles.

4.4 MAC Control Module

The MAC Control Module performs a real-time flow control function for the full duplex operation. Control opcode PAUSE is used for stopping the station that is transmitting the packets. The receive buffer (FIFO) starts to fill up when the upper layer cannot keep up accepting the incoming packets. Before an overflow happens, the upper layer sends a control frame PAUSE to the transmitting station. This control frame inhibits the transmission of the data frames for a specified period of time.

When the MAC Control module receives a PAUSE control frame, it loads the pause timer with the value received in the pause timer value field. The Tx MAC is stopped (paused) from transmitting the data frames for the "pause timer value" slot times. Pause timer decrements one each time a slot time passes by. When the pause time number equals to zero, the MAC transmitter resumes the transmit operation.

The MAC Control Module consists of five modules:

- Control Frame Detector
- Control Frame Generator
- TX/RX MAC Interface
- PAUSE Timer
- Slot Timer

4.4.1 Operation of the Control Frame Detector

Control Frame Detector observes the receiver activity. The incoming data packets are passed through the MAC Control Module to the upper layers while control frames are usually dropped. The PASSALL bit in the MODER register defines whether the control frames are passed or dropped.

A valid PAUSE control frame has the frame structure described on the **Error! Reference source not found.**.

Destination Address (Reserved Multicast address)	Source Address	Length/ Type	Opcode	Pause Timer Value	Reserved	CRC
01-80-c2-00-00-01	xx-xx-xx-xx-xx-xx	8808	0001	xxxx	xxxxxxxxxx	xxxxxxxx
6	6	2	2	2	42	4

64 Bytes

Figure 2: Structure of the PAUSE control frame

Destination address must be a reserved multicast address (01-80-c2-00-00-01) or a destination address equal to the Ethernet IP Core MAC address. The Length/Type field must be equal to 8808 and the opcode must be equal to 0001 for a PAUSE control frame.

When the receive flow control and the MAC Control module are enabled (RXFLOW asserted and PASSALL deasserted), a PAUSE Timer Value from the PAUSE control frame is passed to the PAUSE timer.

4.4.2 Operation of the Control Frame Generator (CFG)

When the host wants to send a PAUSE control frame, it asserts the Transmit Pause Request (TPRQ). When a request is detected, the CFG waits for the current transmission to end. After that the CFG starts to transmit the PAUSE control frame by asserting the Transmit Packet Start Frame (TxPSF), the Transmit Control Frame Flag (TxCFF) and by providing the appropriate control data. TCFF is used for instructing the Transmit function (TX Ethernet MAC) to pad and to append the FCS. The transmit Pause Control Frame End (TxPCFE) is asserted at the end to inform the host that a PAUSE request was send.

Asserting the TXFLOW bit in the MODER register enables the transmission of the PAUSE control frame.

The TPRQ signal (request) is latched in the MAC Control Generator and reset after the PAUSE control frame is transmitted. This prevents issuing a new PAUSE request until the current request is send. The Transmit Pause Timer Value TPTV[15:0] is set prior the transmit pause request is asserted. The TPTV contains the value to be sent as a Pause Timer Value in the pause control frame (Figure 2: Structure of the PAUSE control frame).

4.4.3 Operation of the TX/RX MAC Interface

The MAC Control Module is connected between the host and the Tx/Rx MAC modules. When enabled, the MAC Control module logic takes over the control of the following signals: TxPD[3:0], TxPSF, TxPEF, TxPUD, TxPDN and TxPAB. These signals are connected directly between the host and the MAC transmit and receive functions when data frames are transmitted or received.

On the other hand when a host wants to send a PAUSE control frame it asserts a request signal TPRQ and it is up to MAC Control Module to initiate the transmission. In this case TxPD[3:0], TxPSF, TxPEF, TxPUD, TxPDN and TxPAB are not connected to the host at all. The MAC Control module drives the data signals and instructs the Tx MAC to transmit.

When a PAUSE control frame is received, the frame can be dropped or passed to the host, depending on the state of the PASSALL signal. Again TxPD[3:0], TxPSF, TxPEF, TxPUD, TxPDN and TxPAB are not connected directly.

4.4.4 Operation of the PAUSE Timer

The 16-bit PAUSE timer is loaded with a pause timer value, when a PAUSE control frame is received. The timer inhibits the data frame transmissions for the timer value time slots. This is done by:

- Preventing the Tx MAC module from seeing the signal TxPSF from the host.
- Preventing the host from seeing the signal TxPUD from the Tx MAC Module.

The timer decrements one each time a time slot passes by. A Slot Timer is used for counting the slot time.

4.4.5 Operation of the Slot Timer

Slot timer is activated when a PAUSE Timer is a non-zero. It counts slot times and generates pulses to the PAUSE Timer for every slot time passed.

4.5 MII Management Module

MII Management module is a simple two-wire interface between the host and an external PHY device. It is used for configuration and status read of the physical device. The physical interface consists of a management data line MDIO and a clock line MDC. During the read/write operation the most significant bit is shifted in/out first from/to the MDIO data signal. On each rising edge of the MDC a shift register is shifted to the left and a new value appears on the MDIO.

Internally the interface consists of four signals:

- MDC (Management Data Clock)
- MDI (Management Data Input)
- MDO (Management Data Output)
- MDOEN (Management Data Output Enable)

The unidirectional lines MDI, MDO and MDOEN are combined together to make a bi-directional signal MDIO that is connected to the PHY.

The configuration and status data is written/read to/from the PHY through the MDIO signal.

Management Data Clock MDC is a low frequency clock, derived from the host clock by dividing it.

Three commands are supported for controlling the PHY:

- Write Control Data (Writes the control data to the PHY configuration registers)
- Read Status (Reads the PHY control and status register)
- Scan Status (Continuously reads the PHY status register of one or more PHYs (link fail status)).

The MII Management Module consists of four sub modules:

- Operation Controller
- Shift Registers
- Output Control Module
- Clock Generator

4.5.1 Operation Controller

Operation Controller's task is to perform all supported commands: Write Control Data, Read Status and Scan Status.

4.5.1.1 Write Control Data

A host initiates write operation by asserting the WCTRLDATA signal. When the WCTRLDATA is asserted, that also means that the host data CTLD[15:0], the PHY address FIAD[4:0] and the PHY register address RGAD[4:0] are valid. As soon as the host asserts the WCTRLDATA signal, the MIIM module asserts the BUSY signal to signalize to the host that the write operation is in process. MDOEN is asserted to enable the output line MDO (MDIO) to the PHY. The MIIM module then clocks out the MIIM frame to the PHY on each rising edge of the MDC. The MIIM frame write format conforms to the IEEE 803.2u specification:

- 32-bit long preamble (all ones) if the MIINOPRE bit is not asserted
- 2-bit long Start of frame pattern ST (zero followed by one)

- 2-bit Operation definition (zero-one for write or one-zero for read)
- 5-bit PHY address (FIAD[4:0])
- 5-bit PHY register address RGAD[4:0]
- 2-bit turnaround field TA (one-zero)
- 16-bit data

At the end of the write operation, the BUSY signal is deasserted.

4.5.1.2 Read Status

A host initiates write operation by asserting the RSTAT signal. When RSTAT is asserted, that also means that the PHY address FIAD[4:0] and the PHY register address RGAD[4:0] are valid. As soon as the host asserts the RSTAT signal, the MIIM module asserts the BUSY signal to signalize to the host that the read operation is in process. MDOEN is asserted to enable the output line MDO (MDIO) to the PHY. The MIIM module then clocks out the MIIM frame to the PHY on each rising edge of the MDC and then clocks in the requested data (status). The MIIM read frame format conforms to the IEEE 802.2u specification:

- 32-bit long preamble (all ones) if the MIINOPRE bit is not asserted
- 2-bit long Start of frame pattern ST (zero followed by one)
- 2-bit Operation definition (zero-one for write or one-zero for read)
- 5-bit PHY address (FIAD[4:0])
- 5-bit PHY register address RGAD[4:0]
- 2-bit turnaround field TA (one bit period in which PHY stays in the high-Z state followed by a one-bit period during which the PHY drives a zero on the MDO)
- MIIM deasserts the MDOEN signal that enables the MDI (MDIO works as an input).
- PHY sends the data (status) back to the MIIM module on the data lines PRSD[15:0].

At the end of the read operation, the MIIM deasserts the BUSY signal to indicate to the host that a valid data is on the PRSD[15:0] lines.

4.5.1.3 Scan Status

A host initiates the scan status operation by asserting the SCANSTAT signal. The MIIM performs a continuous read operation of the PHY status register. The PHY is selected by the FIAD[4:0] signals. The link status MIILS signal is asserted/deasserted by the MIIM module and reflects the link status bit of the PHY status register. The signal NVALID is used for qualifying the validity of the MIILS signals and the status data PRSD[15:0]. These signals are invalid until the first scan status operation ends. If the SCANINCR is asserted, the PHY address (FIAD[4:0]) will be incremented after each read, so that link status of many PHYs can be checked sequentially. The PHY with the address equal to FIAD[4:0] will be read first. After each scan status the PHY address will be automatically incremented and next PHY accessed. After the address reaches the maximum value (0x1f), it will be set to the FIAD[4:0] value and the cycle will be repeated. The MIIM drives the SCANPHYADDR[4:0] address lines to indicate to which PHY address was the last scan operation issued.

During the scan status operation, the BUSY signal is asserted until the last read is performed (Scan status operation is stopped).

4.5.2 Operation of the Shift Registers

There are two shift registers in the MII Management Module. Data shift register is used for:

- Shifting out the data to the PHY during the Write Data Control operation
- Shifting in the data during the Read Status operation.
- Shifting out the FIAD[4:0] and the RGAD[4:0] addresses during all operations.

Status shift register contains the data that was latched during the last Read Status Operation. Two additional status signals (Link Status MIILS and Status Invalid NVALID) are latched separately from the Status shift register.

When a Scan Operation is requested, the state of the PRSD[15:0] and a MIILF is constantly updated from the selected PHY register. NVALID is used to for qualifying the validity of the PRSD[15:0] and MIILS signals. These signals are invalid until first scan status operation ends.

4.5.3 Operation of the Output Control Module

Output Control Module combines the MDI, MDO and MDOEN signals into a bi-directional MDIO signal that is connected to the external MII PHY. During the Write Control Data operation the MDIO operates as an output from the MIIM module. The signal is used for transferring data from MIIM module to the PHY. During the Read Status operation the MDIO first operates as an output (addressing the PHY and the PHY internal register) and then as an input to the MIIM module (reading the status data). In both cases the most significant bit of the Data is shifted first. When no operation is performed, the MDIO is tri-stated.

4.5.4 Operation of the Clock Generator

Management Data Clock MDC is a divided host clock. The division factor is set in the MIIMODER register by setting the CLKDIV[7:0] field. (MDC depends on the PHY and can be 2.5 MHz or 12.5 MHz, perhaps something else ☺).

5

Architecture

Ethernet IP Core consists of 5 modules:

- Host Interface and the BD structure
- TX Ethernet MAC (transmit function)
- RX Ethernet MAC (receive function)
- MAC Control Module
- MII Management Module
- Host Interface

5.1 Host Interface and the BD structure

The host interface is connected to the RISC and the external memory through the Wishbone. The RISC writes the data for the configuration registers directly, while the data packets are written to the external memory and just the pointer to that data is passed to the Ethernet Core. This is done with the buffer descriptors (BD).

5.1.1 Host Interface

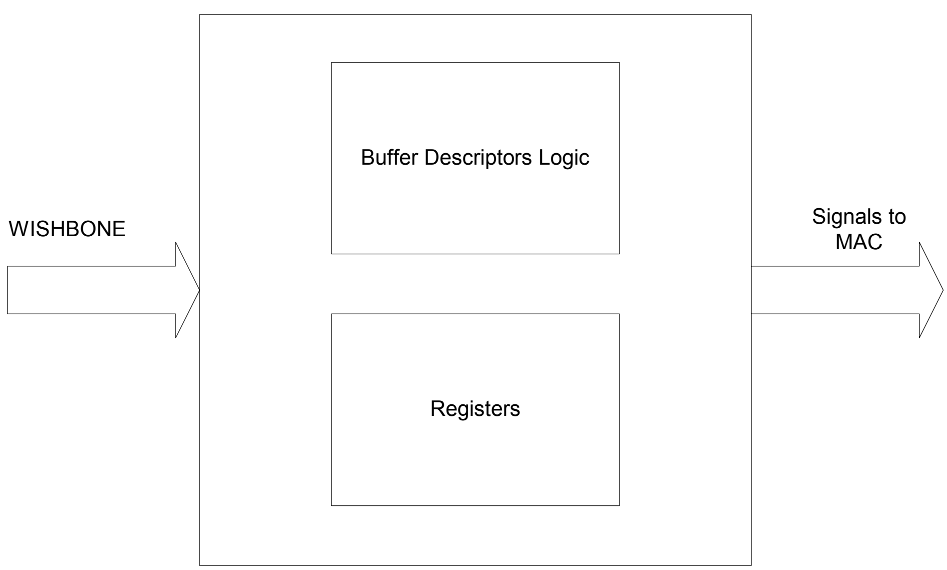


Figure 3: Host Interface

5.1.2 BD Structure

The transmit or receive buffer descriptor consists of:

- Status field (status is written after the BD is used)
- Length field
- Pointer

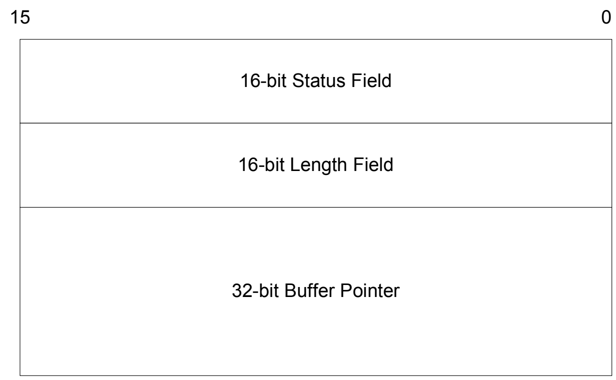


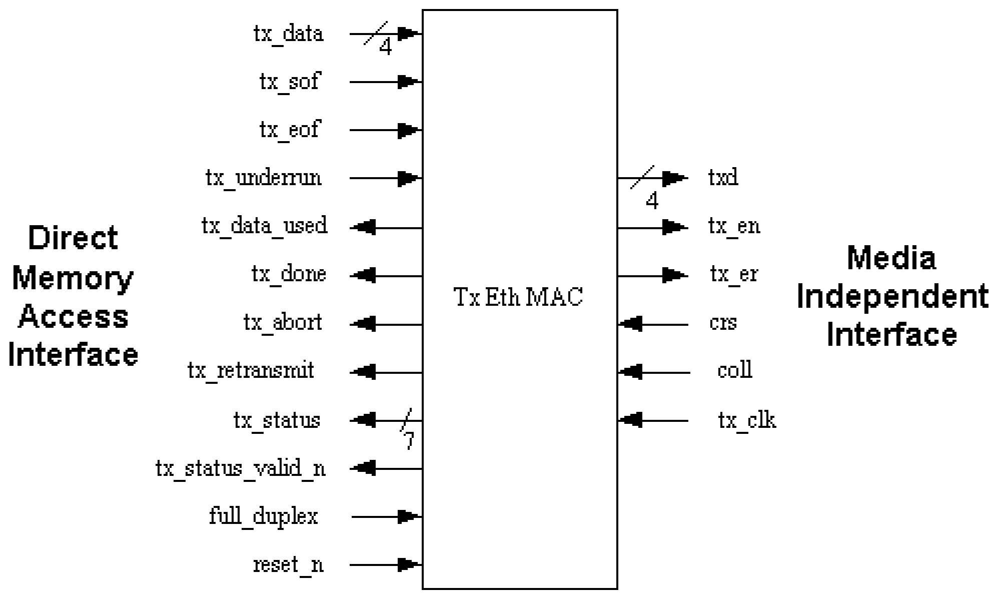
Figure 4: BD Structure

5.2 TX Ethernet MAC

TX Ethernet MAC generates 10BASE-T/100BASE-TX transmit MII nibble data streams in response to the byte streams supplied from the transmit logic (host). It performs the required deferral and Backoff algorithms, takes care for the IPG, computes the checksum (FCS) and monitors the physical media (by monitoring Carrier Sense and collision signals).

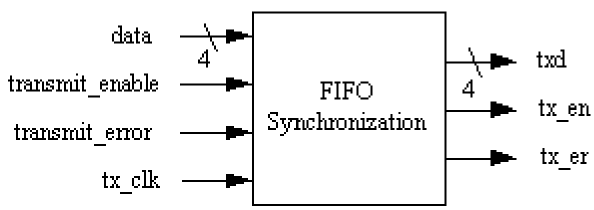
The TX Ethernet MAC consists of eleven sub modules:

- FIFO Synchronization
- IPG (Inter-packet Gap) Timer
- Defer Counter
- Frame Length Counter
- Collision Counter
- Random Number Generator
- Backoff Timer
- Jam Timer
- CRC Generator
- Data Multiplexer
- TX State Machine



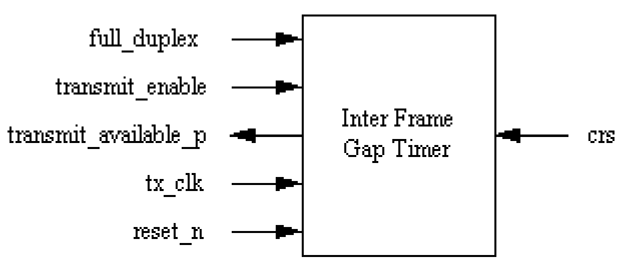
5.2.1 FIFO Synchronization

The function of this module is to keep all outputs synchronous to the rising edge of the input clock.



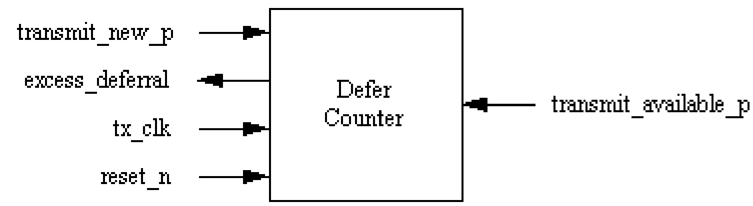
5.2.2 IPG (Inter-Packet Gap) Timer

The function of this module is to assure a minimum time interval between the data packets being transmitted or received.



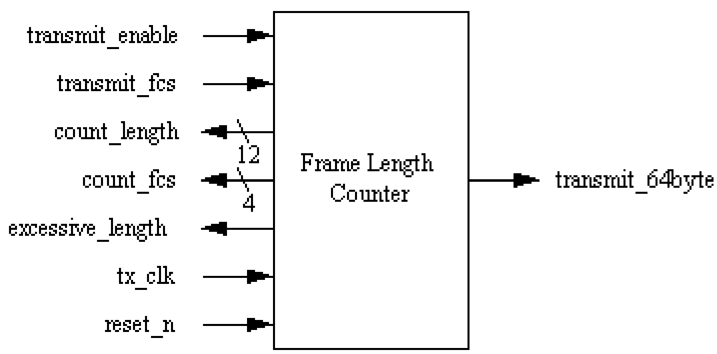
5.2.3 Defer Counter

The function of this module is to limit the defer time for waiting opportunity to transmit a packet of data.



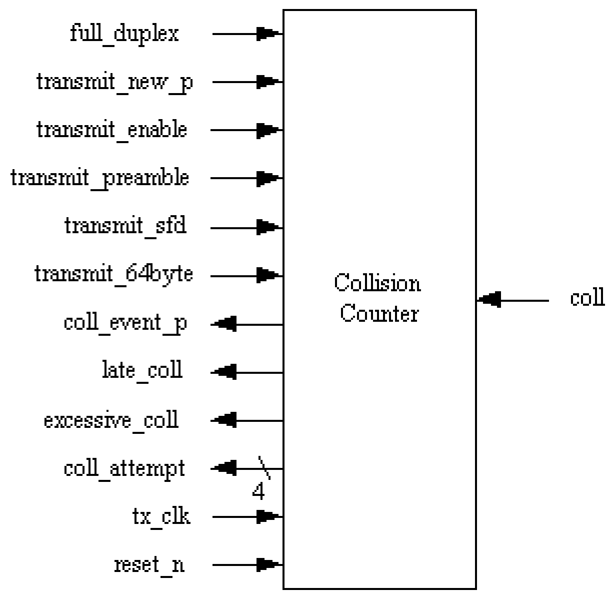
5.2.4 Frame Length Counter

The function of this module is to count the length of frame that is transmitted to the MII.



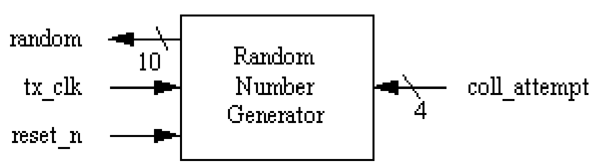
5.2.5 Collision Counter

The function of this module is to count collision events, inspect number of consecutive collisions, and detect late collision.



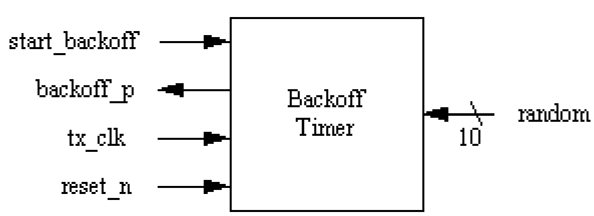
5.2.6 Random Number Generator

This module generates a random number using Linear Feedback Shift Register. The random number is used in back-off module.



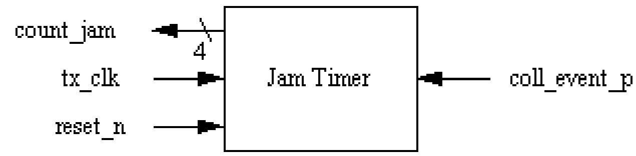
5.2.7 Back off Timer

The function of this module is to determine interval time for backoff operation after a start_backoff is detected.



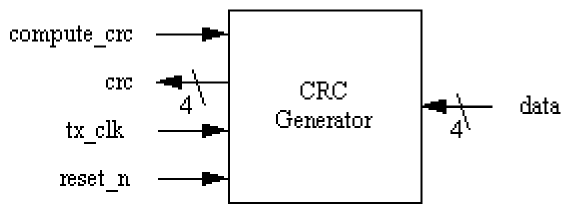
5.2.8 Jam Timer

The function of this module is to determine how long JAM pattern has been transmitted after a collision.



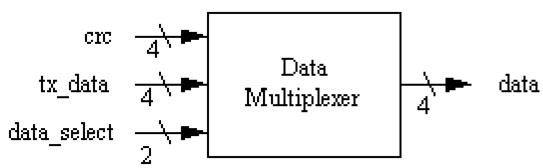
5.2.9 CRC Generator

The function of this module is to generate CRC number, which is added to the Ethernet frame as FCS field.



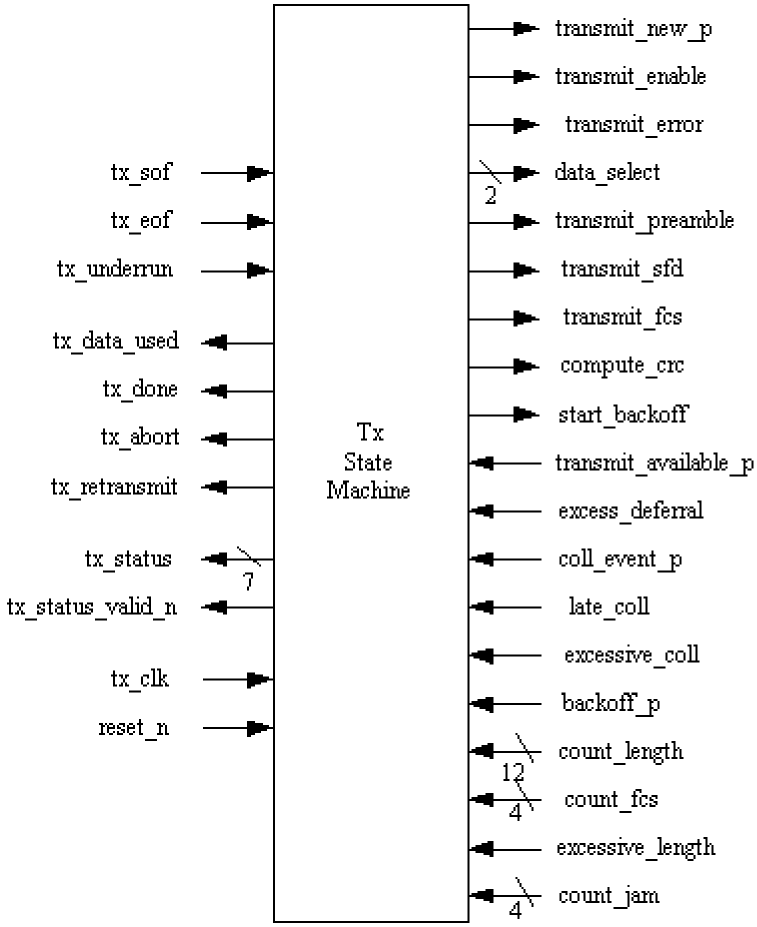
5.2.10 Data Multiplexer

The function of this module is to determine which data nibbles will be transmitted to MII.



5.2.11 TX State Machine

The function of this module is to control the transmit process.

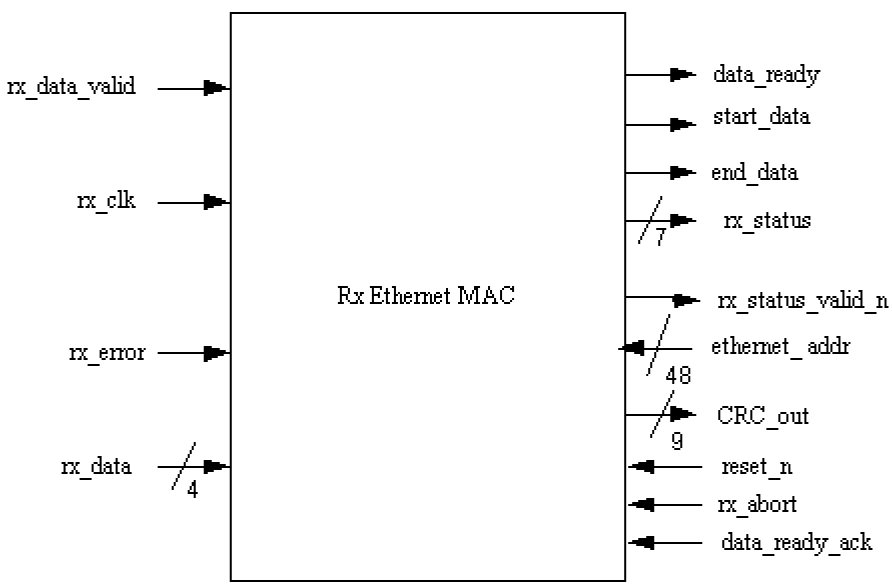

Tx
State
Machine
tx_sof
tx_eof
tx_underrun
tx_data_used
tx_done
tx_abort
tx_retransmit
tx_status
7
tx_status_valid_n
tx_clk
reset_n
transmit_new_p
transmit_enable
transmit_error
data_select
2
transmit_preamble
transmit_sfd
transmit_fcs
compute_crc
start_backoff
transmit_available_p
excess_deferral
coll_event_p
late_coll
excessive_coll
backoff_p
count_length
12
count_fcs
4
excessive_length
count_jam
4

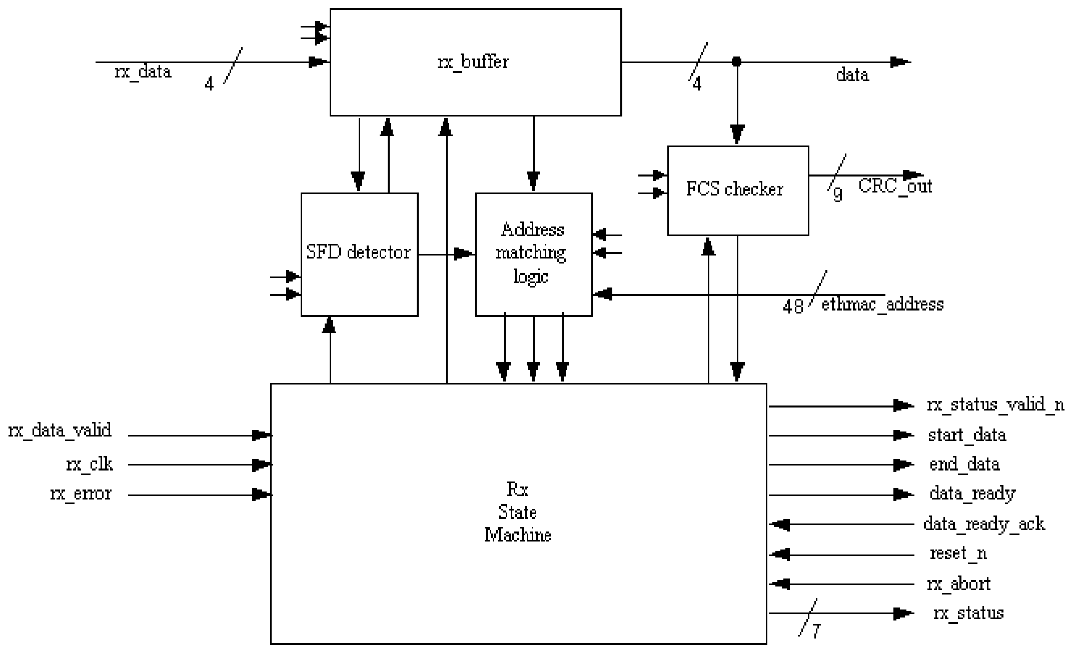
5.3 RX Ethernet MAC

RX Ethernet MAC interprets 10BASE-T/100BASE-TX MII receive data nibble stream and supplies correctly formed packet byte streams to the host. It searches for the SFD (start frame delimiter) at the beginning of the packet, verifies the FCS and detects any dribble nibbles or receive code violations.

The RX Ethernet MAC consists of five modules:

- Rx State Machine
- Rx Buffer
- SFD Detector
- Address Matching Logic
- FCS Checker





5.3.1 Rx State Machine

RX State Machine controls the receive process.

5.3.2 RX Buffer

RX buffer holds the received packet, before it is transferred to FIFO.

5.3.3 SFD Detector

Detects Start Frame Delimiter (SFD) that indicates the start of frame to be received.

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5.3.4 Address Matching Logic

Checks the destination address of the incoming packet, compares it with the Ethernet MAC address and asserts one of the address type signals: broadcast, multicast or individual (address_match).

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5.3.5 FCS Checker

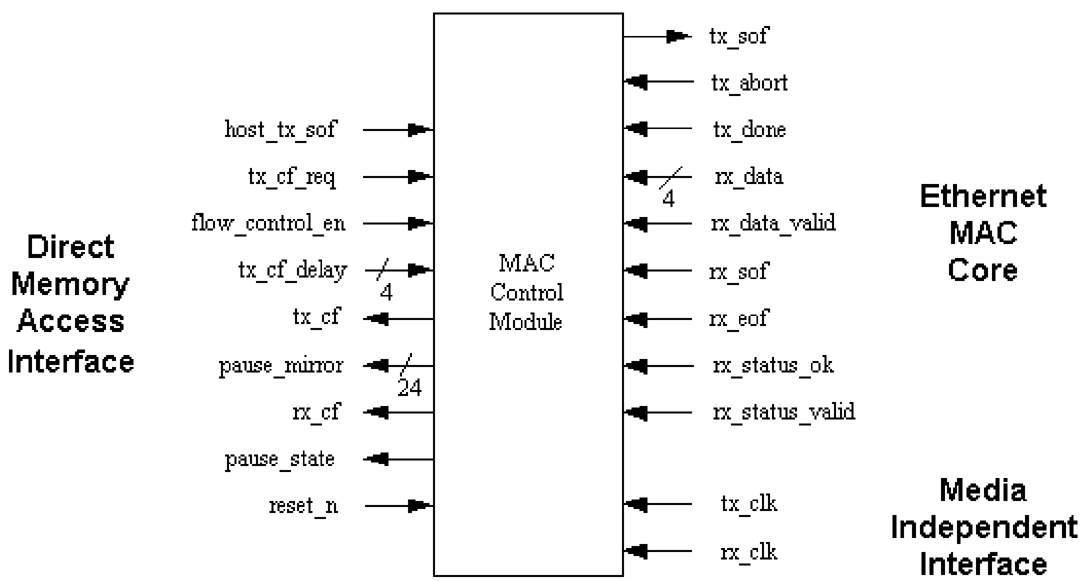
Computes a CRC across the decapsulated frame to find the "magic number" (0xC704DD7B).

5.4 MAC Control Module

The function of this module is to implement the full-duplex flow control.

The MAC Control Module consists of five sub modules:

- Control Frame Detector
- Control Frame Generator
- TX Ethernet MAC Interface
- PAUSE Timer
- Slot Timer



5.4.1 Control Frame Detector

Checks the incoming frames for the control frames. Control frames can be discarded or passed to the host. When a PAUSE control frame is detected, it can stop the Tx MAC from transmitting for a certain period of time.

5.4.2 Control Frame Generator

When there is a need to stop the transmitting station from the transmission (flow control in full duplex mode), a PAUSE control frame can be send to it.

5.4.3 TX Ethernet MAC Interface

MAC Control module is connected between the host interface and the Tx MAC module. Signals from the host are passed by to the Tx MAC in certain occasions and vice versa.

5.4.4 PAUSE Timer

When a PAUSE control frame is received, the pause timer value is written to the PAUSE timer. This prevents the Tx MAC from transmitting for a »pause timer value« period of slot time.

5.4.5 Slot Timer

Slot timer measures time slots and generate a pulse to the PAUSE timer for every slot time passed by.

5.5 MII Management Module

The function of this module is to control the PHY and to gather the information from it (status).

The MII Management Module consists of four sub modules:

- Operation Control Module
- Output Control Module
- Shift Register
- Clock Generator

5.5.1 Operation Control Module

The function of this module is to perform the following commands:

- Write control data
- Read status
- Scan status

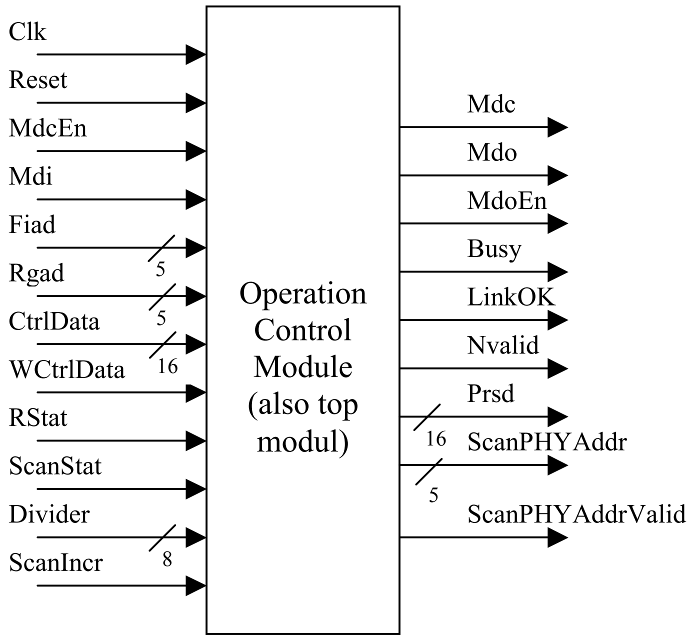


Figure 5: Operation Control Module

5.5.2 Output Control Module

Controls the signal appearance on the MDO, MCK and MDOEN pins.

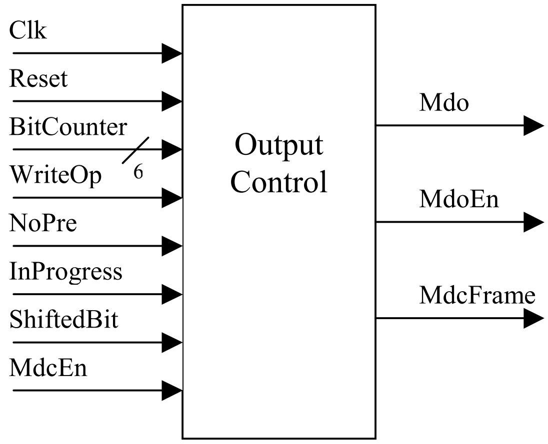


Figure 6: Output Control Module

5.5.3 Shift Register

Holds the status read from an external PHY.

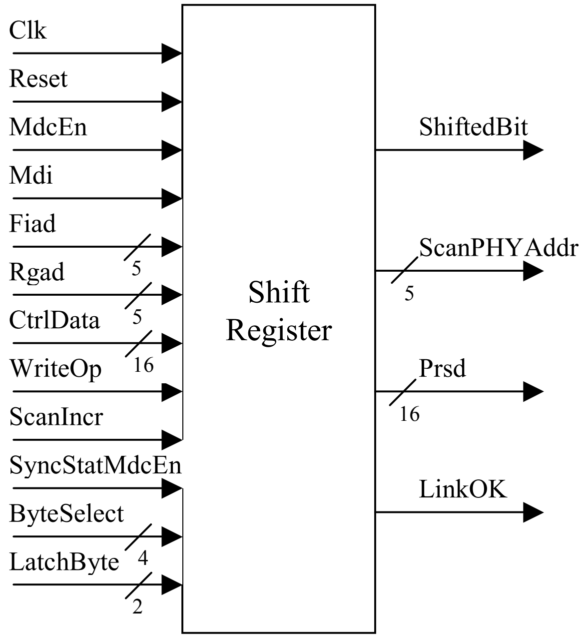


Figure 7: Shift Register

5.5.4 Clock Generator

Generates an appropriate output clock MCK according to the input host clock and the clock divider bits (CLKDIV[7:0] in the MIIMODER register).

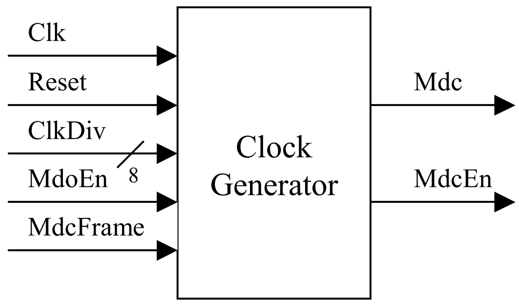


Figure 8: Clock Generator