JT51

The **JT51** is an 8-channel FM sound synthesiser. Each channel is composed of four operators that can be arranged in eight different connections. Vibratto, ADSR envelope and noise are also featured. **JT51** is software compatible with the YM2151 (© Yamaha) and can be embedded in an FPGA as part of a complete music system with special focus in video games and hobby computers.

Pin List

Name	Direction	Width	Description
clk	Input	1	Main clock. Typically 3.58MHz.
rst	Input	1	Reset.
cs_n	Input	1	Chip select. Enables writing to the MMR. Active low.
wr_n	Input	1	Write select. Enables writing to the MMR. Active low. Writing occurs when both cs_n and wr_n are low.
a0	Input	1	0 → Write to MMR selection register 1 → Writes to the location pointed by the selection register
d_in	Input	8	Input data. Only read when cs_n|wr_n==0
d_out	Output	8	Output data. Do not write to JT51 when bit 7 of d_out is high. Bits 0 and 1 indicate overflow of timers A and B.
ct1	Output	1	General purpose output, configurable through MMR.
ct2	Output	1	General purpose output, configurable through MMR.
irq_n	Output	1	Active (low) when timer overflow. Only if programmed to.
p1	Output	1	clk/2. This is the clock at which sound gets synthetised.
sample	Output	1	Indicates that new output data is ready.
left/right	Output	16/16	Audio output with truncated resolution as YM2151. Signed.
xleft/xright	Output	16/16	Audio output with full 16 bit resolution. Signed.
dacleft/ dactright	Output	16/16	Audio output with full 16 bit resolution. Unsigned.

System Design

The top module is called **jt51** and is located in **jt51.v**. All modules, except the timers, are located in separated files with the same name as the module. All jt51_* files are necessary to synthesise the design; as well as some .vh files with look-up tables.

JT51 has separate input and output data lines. The output data is available at all times, even when cs_n is high. The input data is only read when cs_n and wr_n are low at the same time provided **JT51** is not busy. Data written while **JT51** is busy is ignored. The busy status can be checked with the MSB of the d_out bus. Note that a0 only affects to input data. Output data is independent of it.

JT51 can operate at a different speed from the CPU as long as the frequency difference is not as high as to prevent **JT51** from sampling the input data. In general, 8-bit CPUs will operate at the same frequency than **JT51** and 16-bit CPUs will operate at twice the frequency of **JT51**. Sound is synthesised at one half of the **JT51** clock frequency. For the typical case, this means a main clock of 3.5MHz, an internal clock of 1.75MHz and an output data rate of 55kHz, stereo, 16 bits per channel.

The compatible YM2151 had a truncated data output in order to operate with the YM3012 DAC. **JT51** offers an output with the same truncation algorithm. However, the exact outputs (xleft and xright) are the ones recommended to use as they provide better linearity results. These two sets of outputs are 2-complement, signed signals. As some sigma-delta DAC implementations might expect unsigned data, there is one more output set called dacleft/dacright, which removes the sign from the exact output bus.

Test Mode

If the design is synthesised with the macro **TEST_SUPPORT** defined, then register 0x02 has the following meaning:

bit 0 enables envelope test. Regular sound output is replaced by the output of the envelope generator.

bit 1 enables operator 0 test. Only the output of operator 0 is sent out.