Low-Pass IIR (Infinite Impulse Response) Filter IP Core User Manual

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GENERAL INFORMATION

The US_IIR_LP Application Notes contains description of the US_IIR_LP core architecture to explain its proper use.

US_IIR_LP soft core is the unit to perform the Infinite Impulse Responce (IIR) low pass filter which pass frequency is tuned dynamically.

FEATURES

KEY FEATURES

- Dynamically tuned passband cutoff frequency in the range of 0.1 to 0.4 of the sampling frequency. The frequency is set by the 12-bit code with the linear scale.
- using 8-staged wave digital filter scheme of the 33-d order provides both sharp frequency responce – up to 100 db/ octave - and high stopband ripple – up to 80 db. Besides the passband ripple not succedes -2,5%, or –0,23db in the whole frequency range.
- IIR wave digital filters provide both possibility to tune the cutoff frequency and excellent stability.
- Fully pipelined structure provide both high clock frequency – up to 120 MHz, high sampling frequency – up to 15 MHz – and low hardware volume – 960 CLB slices and 3 DSP48 units in Xilinx Virtex2P FPGA device.

DESIGN FEATURES

Usually digital filters are described by the transfer function $H_0(Z)$ which depends on the complex variable Z. This function represents the filtering algorithm with the period L=1 precisely. And each multiplicand Z^k in the function represents the delay to k cycles, which can be implemented on the FIFO with k registers. If the register number in each delay FIFO is increased in n times then the filter with the function $H_n(z) = H_0(Z^n)$ is derived. Such a filter, named the filter with multiple delays, has the following property. Its frequency characteristic is similar to the prototype filter characteristic but in the range of 0 to f_S these characteristic repeats itself n times, where f_S is the quantization frequency.

When the filter stages are connected in a chain then the resulting characteristic is the product of the stage characteristics. When these characteristics are different ones then they mask each other.

Using the masking effect and the stages of filters with multiplied delays the high quality narrow band filters are designed which have small hardware volume.
Besides, in Xilinx FPGAs the multiplied delays are inplemented in FIFO units of SRL16 - type, which occupy the same place as separate registers do.

The fig.2 illustrates the filter computational scheme. The filter consists of 8 stages of the IIR low pass filters which are described by the formula

$$H_{(zK)} = Z^{-2K} + \frac{Z^{-2K} + b(1+a)Z^{-K} + a}{1 + b(1+a)Z^{-K} + aZ^{-2K}} \cdot \frac{Z^{-K} + c}{1 + cZ^{-K}}$$

The exchange of the coefficients b and c provides the tuning of the frequency band.

Additional hardware calkulator performs the calculations of the coefficients b and c providing the linear dependence between input frequency code and cutoff frequency.

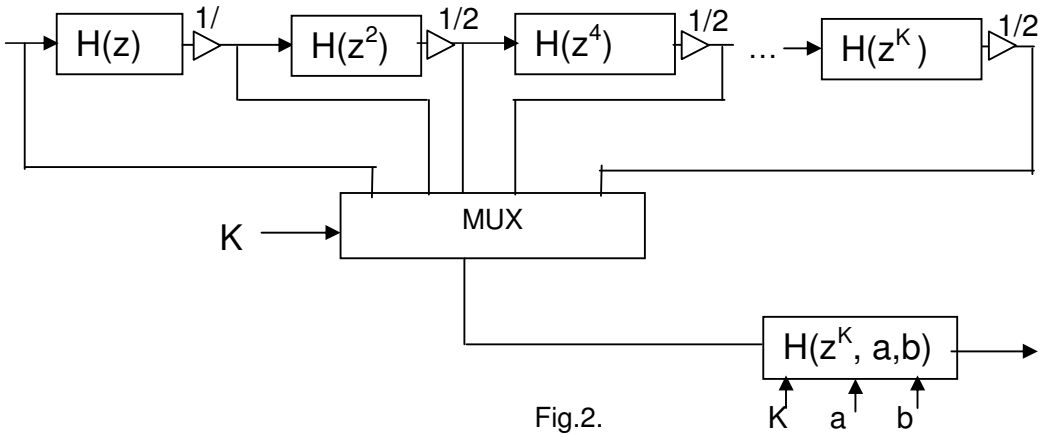

Fig.2.

The filter datapath has the structure of a single filter stage. All the 8 stages are calculated in the sequence. Therefore, the signal sampling frequency is equal to the clock frequency divided to 8.

INTERFACE

SYMBOL

Fig.1 illustrates US_IIR_LP core symbol.

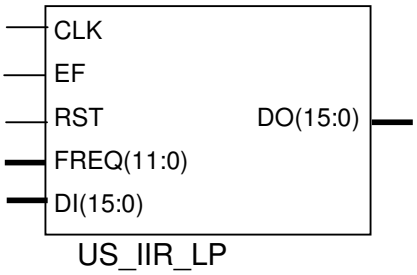

Figure 1. USFFT64 symbol.

SIGNAL DESCRIPTION

The descriptions of the core signals are represented in the table 1.

SIGNAL	TYPE	DESCRIPTION
CLK	input	Global clock
RST	input	Global reset
EF	input	Enabling frequency exchange
FREQ [11:0]	input	Filter frequency code
DI [15:0]	input	Input data sample
DO [15:0]	output	Output data imaginary sample

Table 1. US_IIR_LP core signal description.

Data representation

Input and output data are represented by 16- bit twos complement complex integers.

The frequency code is 12-bit positive integer. The code 4096 represents the sampling frequency divided to 2.

IMPLEMENTATION DATA

PERFORMANCE

The following table 2 illustrates the performance of the US_IIR_LP core

Target device	XC2V4-7	XC 4VSX25-12	XC 5VLX30-3
Area, Slices	716 (23%)	621 (4%)	348 (7%)
Area, DSP48	3(10%)	3(1.5%)	3 (9%)
Maximum system clock	170 MHz	204 MHz	275 MHz

Table 2. Implementation Data – Xilinx Virtex FPGA

Fig 3 illustrates the log magnitude frequency characteristics of the filter for the different frequency codes.

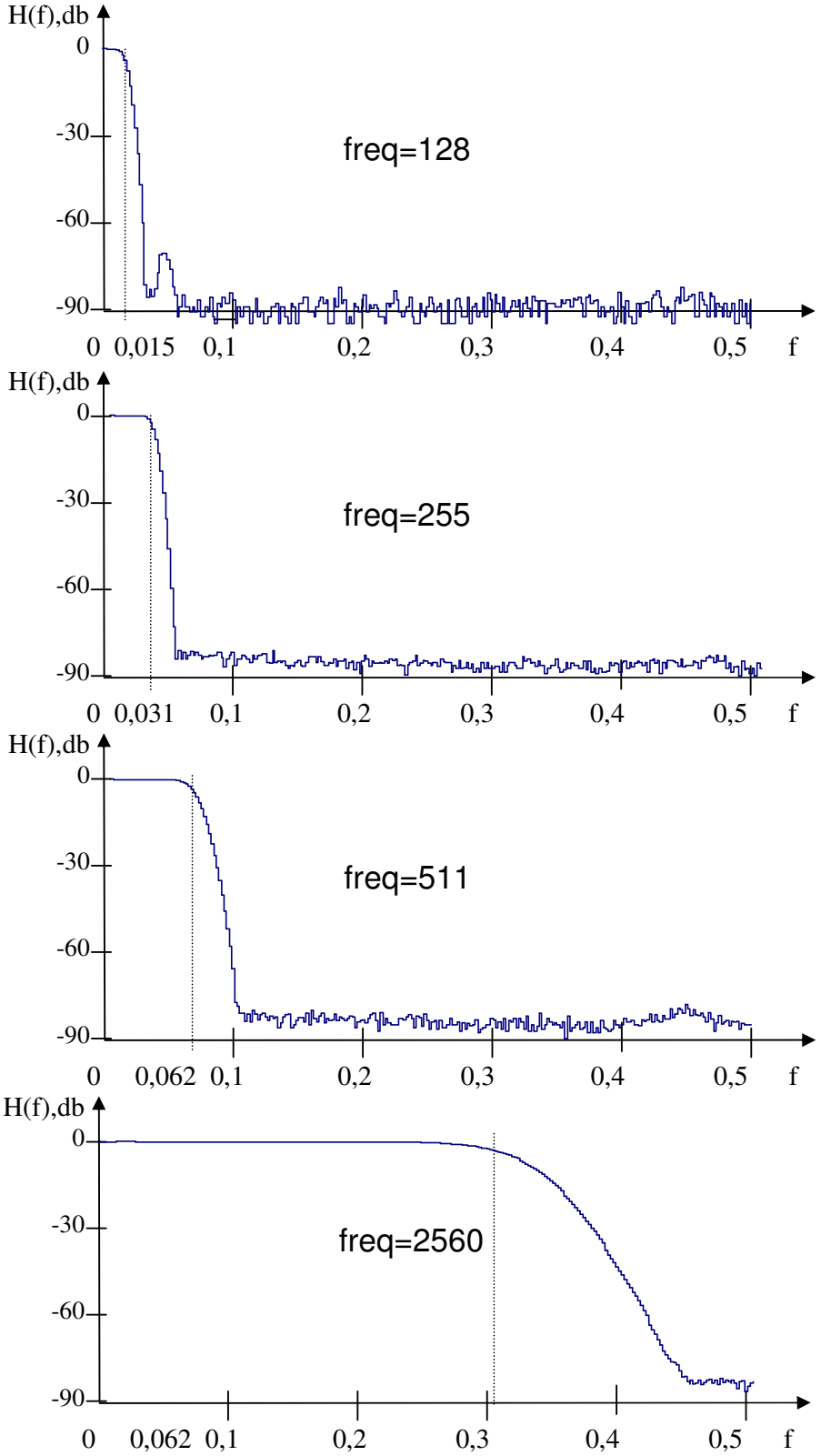

Figure 3. Magnitude-frequency transfer function of US_IIR_LP filter depending on the frequency code freq