

# Chapter 8 *Programming the EPCS Device*

This chapter describes how to program the serial configuration (EPCS) device with Serial Flash Loader (SFL) function via the JTAG interface. Users can program EPCS devices with a JTAG indirect configuration (.jic) file, which is converted from a user-specified SRAM object file (.sof) in Quartus. The .sof file is generated after the project compilation is successful. The steps of converting .sof to .jic in Quartus II are listed below.

# 8.1 Before Programming Begins

The FPGA should be set to AS x1 mode i.e. MSEL[4..0] = "10010" to use the Flash as a FPGA configuration device, as shown in **Figure 8-1**.



Figure 8-1 DIP switch (SW10) setting of Active Serial (AS) mode





# 8.2 Convert .SOF File to .JIC File

 Choose Convert Programming Files from the File menu of Quartus II, as shown in Figure 8-2.

File	Edit View Project	Assignments	Proces
	New	Ctrl+N	
2	Open	Ctrl+O	
	Close	Ctrl+F4	
1	New Project Wizard		
1	Open Project	Ctrl+J	
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	File Properties		
	Create / Update		•
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Figure 8-2 File menu of Quartus II

- 2. Select **JTAG Indirect Configuration File** (.jic) from the **Programming file type** field in the dialog of Convert Programming Files.
- 3. Choose EPCS128 from the Configuration device field.
- 4. Choose Active Serial from the Mode filed.
- 5. Browse to the target directory from the File name field and specify the name of output file.
- 6. Click on the SOF data in the section of Input files to convert, as shown in Figure 8-3.





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Output programming f	file					
Programming file type	: JTAG Indirect Configu	ration File (.jic)			•	]   .
Options	Configuration device:	EPCS128	▼ Mode:	Active S	Serial 🔹 🔻	
File name:	output_file.jic					
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	Create CvP files (G	enerate output_file.periph.	jic and output_file.core.rbf)			
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Input files to convert						51
File/Da	ata area	Properties	Start Address		Add Hex Data	
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SOF Data	Pi	age_U	<auto></auto>		Add File	
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Figure 8-3 Dialog of "Convert Programming Files"

- 7. Click Add File.
- 8. Select the .sof to be converted to a .jic file from the Open File dialog.

#### 9. Click **Open**.

- 10. Click on the Flash Loader and click Add Device, as shown in Figure 8-4.
- 11. Click **OK** and the **Select Devices** page will appear.





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Open Conversion Se	tup Data		Save Conversion S	Setup
Output programming file				
Programming file type: JTAG Indirect Con	figuration File (.jic)			<b></b>
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Create CvP file	s (Generate output_file.periph	.jic and output_file.core.r	bf)	
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DE0_NANO_SOC_Default.sof	5CSEMA4U23			Add Device
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Figure 8-4 Click on the "Flash Loader"

- 12. Select the targeted FPGA to be programed into the EPCS, as shown in Figure 8-5.
- 13. Click **OK** and the **Convert Programming Files** page will appear, as shown in **Figure 8-6**.
- 14. Click Generate.





evice family		Device name	
APEX20K		5CGXFC9D7	▲ New
Arria GX		5CGXFC9E6	
Arria II GX		5CGXFC9E7	Import
Arria II GZ		5CSEBA2	Export
Arria V		5CSEBA4	
Arria V GZ		5CSEBA5	Edit
Cyclone	E	5CSEBA6	Remove
Cydone II		5CSEBA6ES	Keniove
Cyclone III		5CSEMA2	Uncheck All
Cydone III LS		5CSEMA4	
Cydone IV E		5CSEMA5	
Cyclone IV GX		5CSEMA6	
🗹 Cydone V		5CSTFD5D5	
HardCopy II		5CSTFD6D5	
HardCopy III		5CSXFC2C6	E
HardCopy IV		5CSXFC4C6	
MAX 10 FPGA		5CSXFC5C6	
MAX II	+	5CSXFC5D6	Ŧ

Figure 8-5 "Select Devices" page

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onversion setup files					
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utout programming fi	le				
rogramming file types	TTAC Indirect Configu	ration File ( iic)			
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Options	Configuration device:	EPCS128	▼ <u>M</u> ode:	Active Serial	•
le <u>n</u> ame:	output_file.jic				
Advanced	Remote/Local update d	difference file:	DNE		-
	Create Memory Ma	p File (Generate output_file.	map)		
	Create CvP files (G	enerate output_file.periph.ji	ic and output_file.core.rbf)		
	Create config data	RPD (Generate output_file_	auto.rpd)		
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put files to convert	Create config data	RPD (Generate output_file_	auto.rpd)		Add Hay Data
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iput files to convert File/Dar 4 Flash Loader 5CSEMA4	Create config data	RPD (Generate output_file_	auto.rpd) Start Address		Add Hex Data Add Sof Page
File/Dat File/Dat File/Dat Flash Loader 5CSEMA4 SOF Data	Create config data	RPD (Generate output_file_ Properties	auto.rpd) Start Address <auto></auto>		Add Hex Data Add Sof Page Add Device
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Figure 8-6 "Convert Programming Files" page after selecting the device





### 8.3 Write JIC File into the EPCS Device

When the conversion of SOF-to-JIC file is complete, please follow the steps below to program the EPCS device with the .jic file created in Quartus II Programmer.

- 1. Set MSEL[4..0] = "10010"
- 2. Choose Programmer from the Tools menu and the Chain.cdf window will appear.
- **3.** Click **Auto Detect** and then select the correct device(5CSEMA4). Both FPGA device and HPS should be detected, as shown in **Figure 8-7**.
- 4. Double click the red rectangle region shown in **Figure 8-7** and the **Select New Programming File** page will appear. Select the .jic file to be programmed.
- 5. Program the EPCS device by clicking the corresponding **Program/Configure** box. A factory default SFL image will be loaded, as shown in **Figure 8-8**.
- 6. Click **Start** to program the EPCS device.



Figure 8-7 Two devices are detected in the Quartus II Programmer







Figure 8-8 Quartus II programmer window with one .jic file

# 8.4 Erase the EPCS Device

The steps to erase the existing file in the EPCS device are:

- 1. Set MSEL[4..0] = "10010"
- 2. Choose Programmer from the Tools menu and the Chain.cdf window will appear.
- 3. Click Auto Detect, and then select correct device, both FPGA device and HPS will detected. (See Figure 8-7)
- 4. Double click the red rectangle region shown in Figure 8-7, and the Select New **Programming File** page will appear. Select the correct .jic file.
- 5. Erase the EPCS device by clicking the corresponding **Erase** box. A factory default SFL image will be loaded, as shown in **Figure 8-9**.







Figure 8-9 Erase the EPCS device in Quartus II Programmer

6. Click **Start** to erase the EPCS device.

#### 8.5 EPCS Programming via nios-2-flash-programmer

Before programming the EPCS via nios-2-flash-programmer, users must add an EPCS patch file nios-flash-override.txt into the Nios II EDS folder. The patch file is available in the folder Demonstation\EPCS\_Patch of DE0-Nano-SoC System CD. Please copy this file to the folder [QuartusInstalledFolder]\nios2eds\bin (e.g. C:\altera\14.1\nios2eds\bin)

If the patch file is not included into the Nios II EDS folder, an error will occur as shown in **Figure 8-10**.



Figure 8-10 Error Message "No EPCS Layout Data".





# 8.6 Nios II Boot from EPCS Device in Quartus II v14.1

There is a known problem in Quartus II software that the Quartus Programmer must be used to program the EPCS device on DE0-Nano-SoC board.

Please refer to Altera's website here with details step by step.

