Programmable 3-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V and 3.3-V LVCMOS Outputs

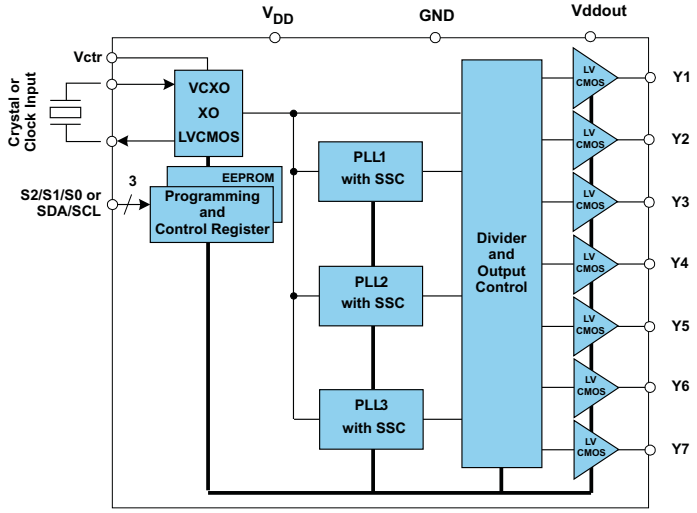
Check for Samples: CDCE937, CDCEL937

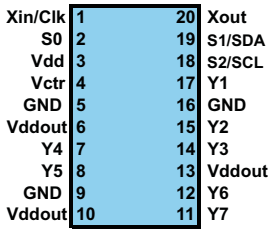
FEATURES

- Member of Programmable Clock Generator Family
  - CDCE913/CDCEL913: 1-PLL, 3 Outputs
  - CDCE925/CDCEL925: 2-PLL, 5 Outputs
  - *CDCE937/CDCEL937: 3-PLL, 7 Outputs*
  - CDCE949/CDCEL949: 4-PLL, 9 Outputs
- In-System Programmability and EEPROM
  - Serial Programmable Volatile Register
  - Nonvolatile EEPROM to Store Customer Setting
- Flexible Input Clocking Concept
  - External Crystal: 8 MHz to 32 MHz
  - On-Chip VCXO: Pull Range ±150 ppm
  - Single-Ended LVCMOS up to 160 MHz
- Selectable Output Frequency up to 230 MHz
- Low-Noise PLL Core
  - Integrated PLL Loop Filter Components
  - Low Period Jitter (Typ 60 ps)
- Separate Output Supply Pins
  - CDCE937: 3.3 V and 2.5 V
  - CDCEL937: 1.8 V
- 1.8-V Device Power Supply
- Flexible Clock Driver
  - Three User-Definable Control Inputs [S0/S1/S2] e.g., SSC Selection, Frequency Switching, Output Enable or Power Down
  - Generates Highly Accurate Clocks for Video, Audio, USB, IEEE1394, RFID, Bluetooth™, WLAN, Ethernet™, and GPS
  - Generates Common Clock Frequencies Used With TI DaVinci™, OMAP™, DSPs
  - Programmable SSC Modulation
  - Enables 0-PPM Clock Generation
- Wide Temperature Range –40° C to 85° C
- Packaged in TSSOP
- Development and Programming Kit for Easy PLL Design and Programming (TI Pro-Clock™)

APPLICATIONS

- D-TV, HD-TV, STB, IP-STB, DVD-Player, DVD-Recorder, Printer





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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The CDCE937 and CDCEL937 are modular PLL-based low cost, high-performance, programmable clock synthesizers, multipliers and dividers. They generate up to 7 output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using up to three independent configurable PLLs.

The CDCx937 has separate output supply pins, VDDOUT, which is 1.8 V for CDCEL937 and to 2.5 V to 3.3 V for CDCE937.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF. Additionally, an on-chip VCXO is selectable which allows synchronization of the output frequency to an external control signal, that is, PWM signal.

The deep M/N divider ratio allows the generation of zero ppm audio/video, networking (WLAN, BlueTooth, Ethernet, GPS) or Interface (USB, IEEE1394, Memory Stick) clocks from a reference input frequency such as 27 MHz.

All PLLs supports SSC (Spread-Spectrum Clocking). SSC can be Center-Spread or Down-Spread clocking which is a common technique to reduce electro-magnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic of each PLL.

The device supports non-volatile EEPROM programming for ease-customized application. It is preset to a factory default configuration (see the *Default Device Configuration* section). It can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through SDA/SCL bus, a 2-wire serial interface.

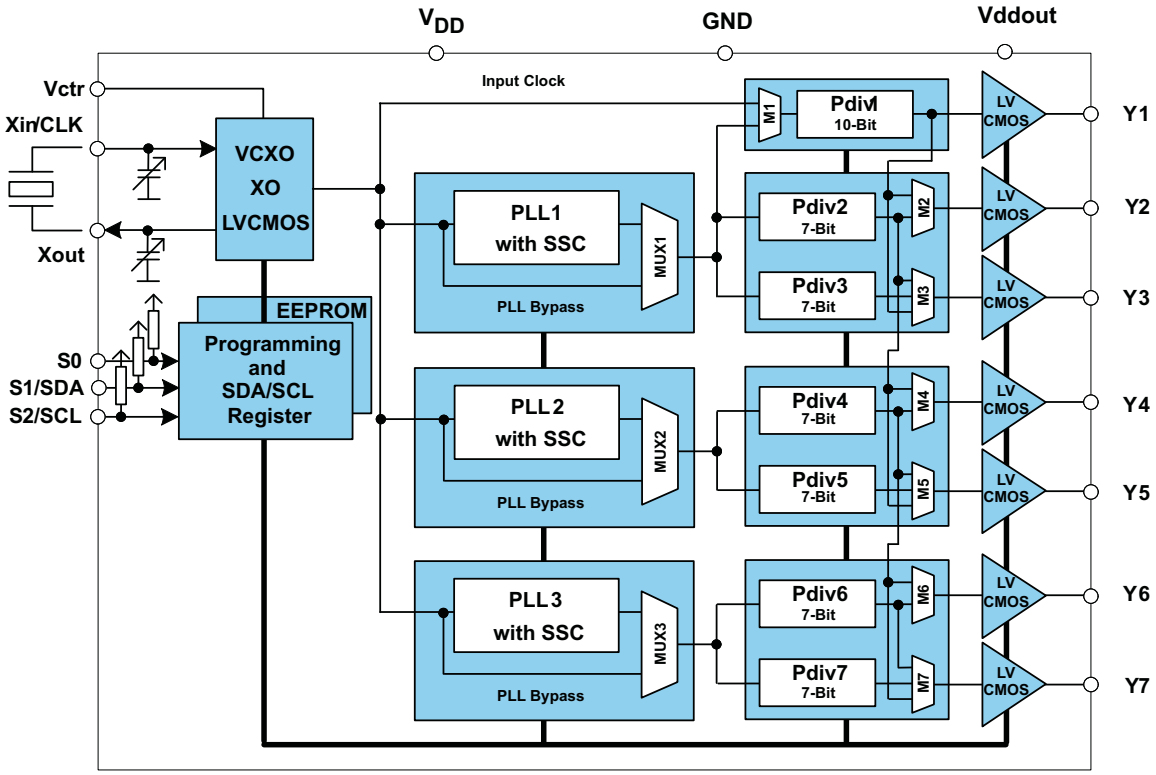
Three programmable control inputs, S0, S1 and S2, can be used to control various aspects of operation including frequency selection changing the SSC parameters to lower EMI, PLL bypass, power down, and choosing between low level or 3-state for output-disable function.

The CDCx937 operates in 1.8 V environment. It is characterized for operation from –40°C to 85°C.

Terminal Functions for CDCE937, CDCEL937

NAME	PIN TSSOP24	TYPE	DESCRIPTION
Y1, Y2, ... Y7	17, 15, 14, 7, 8, 12, 11	O	LVCMOS outputs
Xin/CLK	1	I	Crystal Oscillator Input or LVCMOS Clock Input (selectable via SDA/SCL bus)
Xout	20	O	Crystal Oscillator Output (leave open or pull-up (~500k) when not used)
V_{Ctrl}	4	I	VCXO Control Voltage (leave open or pull-up (~500k) when not used)
V_{DD}	3	Power	1.8V Power Supply for the device
Vddout	6, 10, 13	Power	**CDCEL937:** 1.8V Supply for all Outputs
			CDCE937: 3.3V or 2.5V Supply for all Outputs
GND	5, 9, 16	Ground	Ground
S0	2	I	User Programmable Control Input S0; LVCMOS inputs; Internal Pull-up 500k
SDA/S1	19	I/O or I	**SDA:** Bi-Directional Serial Data Input/Output (default configuration). LVCMOS; Internal Pull-up 500k; or **S1:** User Programmable Control Input; LVCMOS inputs; Internal Pull-up 500k
SCL/S2	18	I	**SCL:** Serial Clock Input(default configuration), LVCMOS; Internal Pull-up 500k; or **S2:** User Programmable Control Input; LVCMOS inputs; Internal Pull-up 500k

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 2.5	V
V_I	Input voltage range(2) (3)	–0.5 to V_{DD} + 0.5	V
V_O	Output voltage range(2)	–0.5 to Vddout + 0.5	V
I_I	Input current (V_I < 0, V_I > V_{DD})	20	mA
I_O	Continuous output current	50	mA
T_{stg}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) SDA and SCL can go up to 3.6V as stated in the *Recommended Operating Conditions* table.

PACKAGE THERMAL RESISTANCE for TSSOP (PW) PACKAGE(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		AIRFLOW (lfm)	TSSOP20 °C/W
T_{JA}	Thermal Resistance Junction to Ambient	0	89
		150	75
		200	74
		250	74
		500	69
T_{JC}	Thermal Resistance Junction to Case	—	31
T_{JB}	Thermal Resistance Junction to Board	—	55
$R_{\theta JT}$	Thermal Resistance Junction to Top	—	0.8
$R_{\theta JB}$	Thermal Resistance Junction to Bottom	—	49

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.7	1.8	1.9	V
V_O	Output Yx supply voltage for CDCE937, Vddout	2.3		3.6	
	Output Yx supply voltage for CDCEL937, Vddout	1.7		1.9	V
V_{IL}	Low-level input voltage LVCMOS			0.3 V_{DD}	V
V_{IH}	High-level input voltage LVCMOS	0.7 V_{DD}			V
$V_{I(thresh)}$	Input voltage threshold LVCMOS		0.5 V_{DD}		V
V_{IS}	Input voltage range S0	0		1.9	V
	Input voltage range S1, S2, SDA, SCL; $V_{I(thresh)}$ = 0.5 V_{DD}	0		3.6	
$V_{I(CLK)}$	Input voltage range CLK	0		1.9	V
I_{OH} /I_{OL}	Output current (Vddout = 3.3 V)			±12	mA
	Output current (Vddout = 2.5 V)			±10	
	Output current (Vddout = 1.8 V)			±8	
C_L	Output load LVCMOS			10	pF
T_A	Operating free-air temperature	–40		85	°C

RECOMMENDED CRYSTAL/VCXO SPECIFICATIONS(1)

		MIN	NOM	MAX	UNIT
f_{Xtal}	Crystal input frequency range (fundamental mode)	8	27	32	MHz
ESR	Effective series resistance			100	Ω
f_{PR}	Pulling range (0 V ≤ Vctrl ≤ 1.8 V)(2)	±120	±150		ppm
	Frequency control voltage, Vctrl	0		V_{DD}	V
C_0/C_1	Pullability ratio			220	
C_L	On-chip load capacitance at Xin and Xout	0		20	pF

(1) For more information about VCXO configuration, and crystal recommendation, see application report (SCAA085).
(2) Pulling range depends on crystal-type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of min ±120 ppm applies for crystal listed in the application report (SCAA085).

EEPROM SPECIFICATION

		MIN	TYP	MAX	UNIT
EEcyc	Programming cycles of EEPROM	1000			cycles
EEret	Data retention	10			years

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature

			MIN	NOM	MAX	UNIT
CLK_IN REQUIREMENTS						
f_{CLK}	LVCMOS clock input frequency	PLL bypass mode	0		160	MHz
		PLL mode	8		160	
t_r / t_f	Rise and fall time CLK signal (20% to 80%)				3	ns
$duty_{CLK}$	Duty cycle CLK at V_{DD}/2		40%		60%	

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
SDA/SCL TIMING REQUIREMENTS (see Figure 12)						
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{su(START)}$	START setup time (SCL high before SDA low)	4.7		0.6		µs
$t_{h(START)}$	START hold time (SCL low after SDA low)	4		0.6		µs
$t_{w(SCLL)}$	SCL low-pulse duration	4.7		1.3		µs
$t_{w(SCLH)}$	SCL high-pulse duration	4		0.6		µs
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	0	3.45	0	0.9	µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
t_r	SCL/SDA input rise time		1000		300	ns
t_f	SCL/SDA input fall time		300		300	ns
$t_{su(STOP)}$	STOP setup time	4		0.6		µs
t_{BUS}	Bus free time between a STOP and START condition	4.7		1.3		µs

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
OVERALL PARAMETER							
I_{DD}	Supply current (see Figure 3)	All outputs off, $f_{(CLK)}$ = 27 MHz, $f_{(VCO)}$ = 135 MHz	All PLLS on		29		mA
			Per PLL		9		
I_{DDOUT}	Output supply current (see Figure 4 and Figure 5	No load, all outputs on, f_{OUT} = 27 MHz	CDCE937, V_{DDOUT} = 3.3 V		3.1		mA
			CDCEL937, V_{DDOUT} = 1.8 V		1.5		
$I_{DD(PD)}$	Power-down current. Every circuit powered down except SDA/SCL	f_{IN} = 0 MHz,	V_{DD} = 1.9 V		50		µA
$V_{(PUC)}$	Supply voltage Vdd threshold for power-up control circuit			0.85		1.45	V
$f_{(VCO)}$	VCO frequency range of PLL			80		230	MHz
f_{OUT}	LVCMOS output frequency	Vddout = 3.3 V		230			MHz
		Vddout = 1.8 V		230			
LVCMOS PARAMETER							
V_{IK}	LVCMOS input voltage	V_{DD} = 1.7 V; I_I = –18 mA				–1.2	V
I_I	LVCMOS Input current	VI = 0 V or V_{DD}; V_{DD} = 1.9 V				±5	µA
I_{IH}	LVCMOS Input current for S0/S1/S2	V_I = V_{DD}; V_{DD} = 1.9 V				5	µA
I_{IL}	LVCMOS Input current for S0/S1/S2	V_I = 0 V; V_{DD} = 1.9 V				–4	µA
C_I	Input capacitance at Xin/Clk	$V_{I(Clk)}$ = 0 V or V_{DD}			6		pF
	Input capacitance at Xout	$V_{I(Xout)}$ = 0 V or V_{DD}			2		
	Input capacitance at S0/S1/S2	V_{IS} = 0 V or V_{DD}			3		
CDCE937 - LVCMOS PARAMETER FOR Vddout = 3.3 V – MODE							
V_{OH}	LVCMOS high-level output voltage	Vddout = 3 V, I_{OH} = –0.1 mA		2.9			V
		Vddout = 3 V, I_{OH} = –8 mA		2.4			
		Vddout = 3 V, I_{OH} = –12 mA		2.2			
V_{OL}	LVCMOS low-level output voltage	Vddout = 3 V, I_{OL} = 0.1 mA				0.1	V
		Vddout = 3 V, I_{OL} = 8 mA				0.5	
		Vddout = 3 V, I_{OL} = 12 mA				0.8	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass			3.2		ns
t_r/t_f	Rise and fall time	Vddout= 3.3 V (20%–80%)			0.6		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3			60	90	ps
		3 PLL switching, Y2-to-Y7			100	150	
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3			70	100	ps
		3 PLL switching, Y2-to-Y7			120	180	
$t_{sk(o)}$	Output skew (4) , See Table 2	f_{OUT} = 50 MHz; Y1-to-Y3				60	ps
		f_{OUT} = 50 MHz; Y2-to-Y5				160	
odc	Output duty cycle (5)	f_{VCO} = 100 MHz; Pdiv = 1		45%		55%	

(1) All typical values are at respective nominal V_{DD}.
(2) 10000 cycles.
(3) Jitter depends on configuration. Data is taken under the following conditions: 1-PLL : f_{IN} = 27MHz, Y2/3 = 27 MHz, (measured at Y2), 3-PLL: f_{IN} = 27 MHz, Y2/3 = 27 MHz (measured at Y2), Y4/5 = 16.384 MHz, Y6/7 = 74.25 MHz
(4) The tsk(o) specification is only valid for equal loading of each bank of outputs, and outputs are generated from the same divider; data taking on rising edge (tr).
(5) odc depends on output rise and fall time (t_r/t_f).

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CDCE937 – LVCMOS PARAMETER for Vddout = 2.5 V – Mode						
V_{OH}	LVCMOS high-level output voltage	Vddout = 2.3 V, I_{OH} = –0.1 mA	2.2			V
		Vddout = 2.3 V, I_{OH} = –6 mA	1.7			
		Vddout = 2.3 V, I_{OH} = –10 mA	1.6			
V_{OL}	LVCMOS low-level output voltage	Vddout = 2.3 V, I_{OL} = 0.1 mA			0.1	V
		Vddout = 2.3 V, I_{OL} = 6 mA			0.5	
		Vddout = 2.3 V, I_{OL} = 10 mA			0.7	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass		3.4		ns
t_r/t_f	Rise and fall time	Vddout = 2.5 V (20%–80%)		0.8		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(6) (7)	1 PLL switching, Y2-to-Y3		60	90	ps
		3 PLL switching, Y2-to-Y7		100	150	
$t_{jit(per)}$	Peak-to-peak period jitter(8)	1 PLL switching, Y2-to-Y3		70	100	ps
		3 PLL switching, Y2-to-Y7		120	180	
$t_{sk(o)}$	Output skew(8), See Table 2	f_{OUT} = 50 MHz; Y1-to-Y3			60	ps
		f_{OUT} = 50 MHz; Y2-to-Y5			160	
odc	Output duty cycle(9)	$f_{(VCO)}$ = 100 MHz; Pdiv = 1	45%		55%	
CDCEL937 — LVCMOS PARAMETER for Vddout = 1.8 V – Mode						
V_{OH}	LVCMOS high-level output voltage	Vddout = 1.7 V, I_{OH} = –0.1 mA	1.6			V
		Vddout = 1.7 V, I_{OH} = –4 mA	1.4			
		Vddout = 1.7 V, I_{OH} = –8 mA	1.1			
V_{OL}	LVCMOS low-level output voltage	Vddout = 1.7 V, I_{OL} = 0.1 mA			0.1	V
		Vddout = 1.7 V, I_{OL} = 4 mA			0.3	
		Vddout = 1.7 V, I_{OL} = 8 mA			0.6	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass		2.6		ns
t_r/t_f	Rise and fall time	Vddout= 1.8 V (20%–80%)		0.7		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(6) (7)	1 PLL switching, Y2-to-Y3		70	120	ps
		3 PLL switching, Y2-to-Y7		100	150	
$t_{jit(per)}$	Peak-to-peak period jitter(7)	1 PLL switching, Y2-to-Y3		90	140	ps
		3 PLL switching, Y2-to-Y7		120	190	
$t_{sk(o)}$	Output skew(8), See Table 2	f_{OUT} = 50 MHz; Y1-to-Y3			60	ps
		f_{OUT} = 50 MHz; Y2-to-Y5			160	
odc	Output duty cycle(9)	$f_{(VCO)}$ = 100 MHz; Pdiv = 1	45%		55%	
SDA/SCL PARAMETER						
V_{IK}	SCL and SDA input clamp voltage	V_{DD} = 1.7 V; I_I = –18 mA			–1.2	V
I_{IH}	SCL and SDA input current	V_I = V_{DD}; V_{DD} = 1.9 V			±10	μA
V_{IH}	SDA/SCL input high voltage(10)		0.7 V_{DD}			V
V_{IL}	SDA/SCL input low voltage(10)				0.3 V_{DD}	V
V_{OL}	SDA low-level output voltage	I_{OL} = 3 mA, V_{DD} = 1.7 V			0.2 V_{DD}	V
C_I	SCL/SDA Input capacitance	V_I = 0 V or V_{DD}		3	10	pF

(6) 10000 cycles.
(7) Jitter depends on configuration. Data is taken under the following conditions: 1-PLL : f_{IN} = 27MHz, Y2/3 = 27 MHz, (measured at Y2), 3-PLL: f_{IN} = 27 MHz, Y2/3 = 27 MHz (measured at Y2), Y4/5 = 16.384 MHz, Y6/7 = 74.25 MHz
(8) The tsk(o) specification is only valid for equal loading of each bank of outputs, and outputs are generated from the same divider; data taking on rising edge (tr).
(9) odc depends on output rise and fall time (t_r/t_f).
(10) SDA and SCL pins are 3.3 V tolerant.

PARAMETER MEASUREMENT INFORMATION

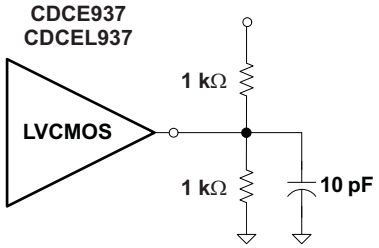


Figure 1. Test Load

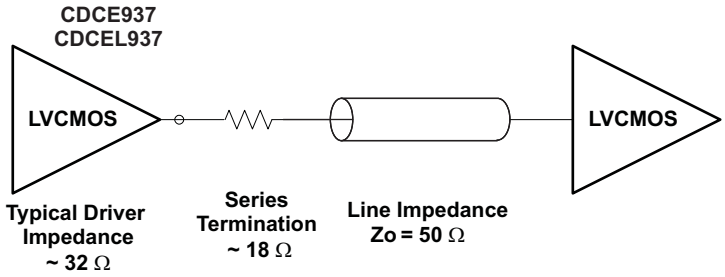


Figure 2. Test Load for 50-Ω Board Environment

TYPICAL CHARACTERISTICS

CDCE937, CDCEL937
SUPPLY CURRENT
vs
PLL FREQUENCY

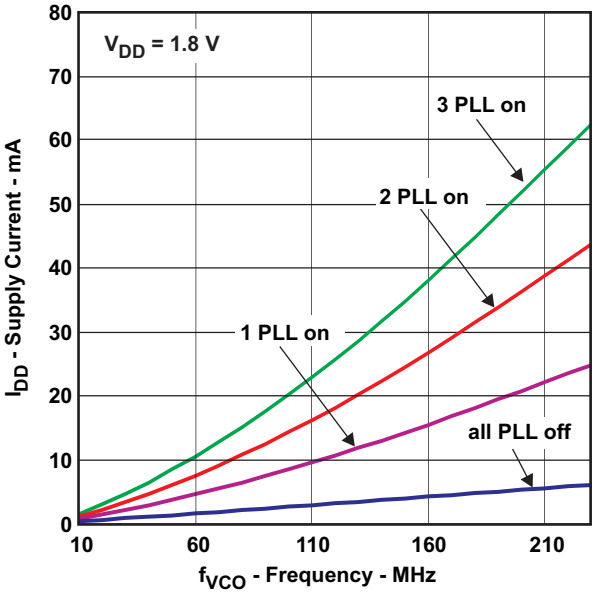


Figure 3.

CDCE937
OUTPUT CURRENT
vs
OUTPUT FREQUENCY

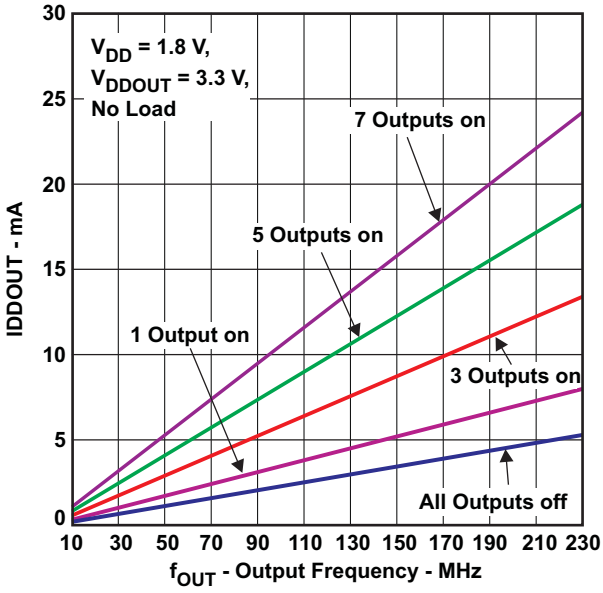


Figure 4.

CDCEL937
OUTPUT CURRENT
vs
OUTPUT FREQUENCY

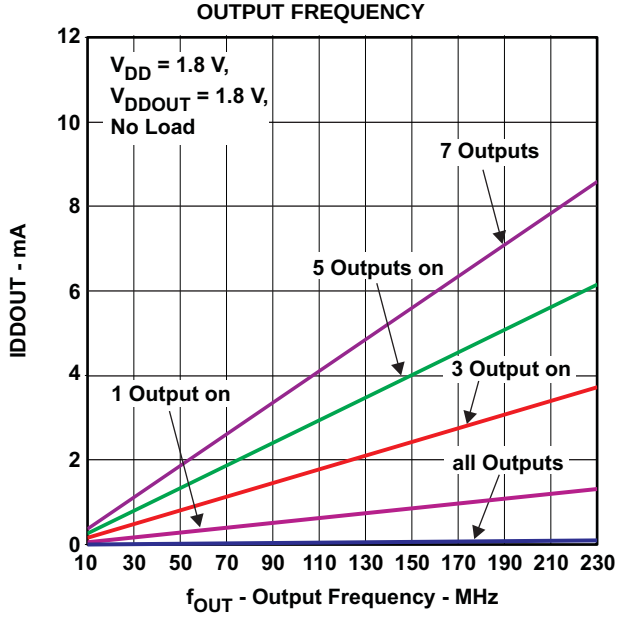


Figure 5.

APPLICATION INFORMATION

CONTROL TERMINAL SETTING

The CDCE937/CDCEL937 has three user-definable control terminals (S0, S1, and S2) which allow external control of device settings. They can be programmed to any of the following setting:

- Spread spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power down control

The user can predefine up to eight different control settings. Table 1 and Table 2 explain these settings.

Table 1. Control Terminal Definition

External Control Bits	PLL1 Setting			PLL2 Setting			PLL3 Setting			Y1 Setting
Control Function	PLL Frequency Selection	SSC Selection	Output Y2/Y3 Selection	PLL Frequency Selection	SSC Selection	Output Y4/Y5 Selection	PLL Frequency Selection	SSC Selection	Output Y6/Y7 Selection	Output Y1 and Power-Down Selection

Table 2. PLLx Setting (can be selected for each PLL individual)(1)

SSC Selection (Center/Down)				
SSCx [3-bits]			Center	Down
0	0	0	0% (off)	0% (off)
0	0	1	±0.25%	–0.25%
0	1	0	±0.5%	–0.5%
0	1	1	±0.75%	–0.75%
1	0	0	±1.0%	–1.0%
1	0	1	±1.25%	–1.25%
1	1	0	±1.5%	–1.5%
1	1	1	±2.0%	–2.0%
FREQUENCY SELECTION(2)				
FSx			**FUNCTION**	
0			Frequency0	
1			Frequency1	
OUTPUT SELECTION(3) (Y2 ... Y7)				
YxYx			**FUNCTION**	
0			State0	
1			State1	

(1) Center/Down-Spread, Frequency0/1 and State0/1 are user-definable in PLLx Configuration Register;
(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.
(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, 3-state, low or active

Table 3. Y1 Setting(1)

Y1 SELECTION	
Y1	**FUNCTION**
0	State 0
1	State 1

(1) State0 and State1 are user definable in Generic Configuration Register and can be power down, 3-state, low, or active.

S1/SDA and S2/SCL pins of the CDCE937/CDCEL937 are dual function pins. In default configuration they are defined as SDA/SCL for the serial interface. They can be programmed as control-pins (S1/S2) by setting the relevant bits in the EEPROM. Note that the changes to the Control register (Bit [6] of Byte [02]) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control-pins, S1 and S2, temporally act as serial programming pins (SDA/SCL).

S0 is not a multi-use pin, it is a control pin only.

DEFAULT DEVICE SETTING

The internal EEPROM of CDCE937/CDCEL937 is preconfigured as shown in Figure 6. (The input frequency is passed through to the output as a default). This allows the device to operate in default mode without the extra production step of program it. The default setting appears after power is supplied or after power-down/up sequence until it is re-programmed by the user to a different application configuration. A new register setting is programmed via the serial SDA/SCL Interface.

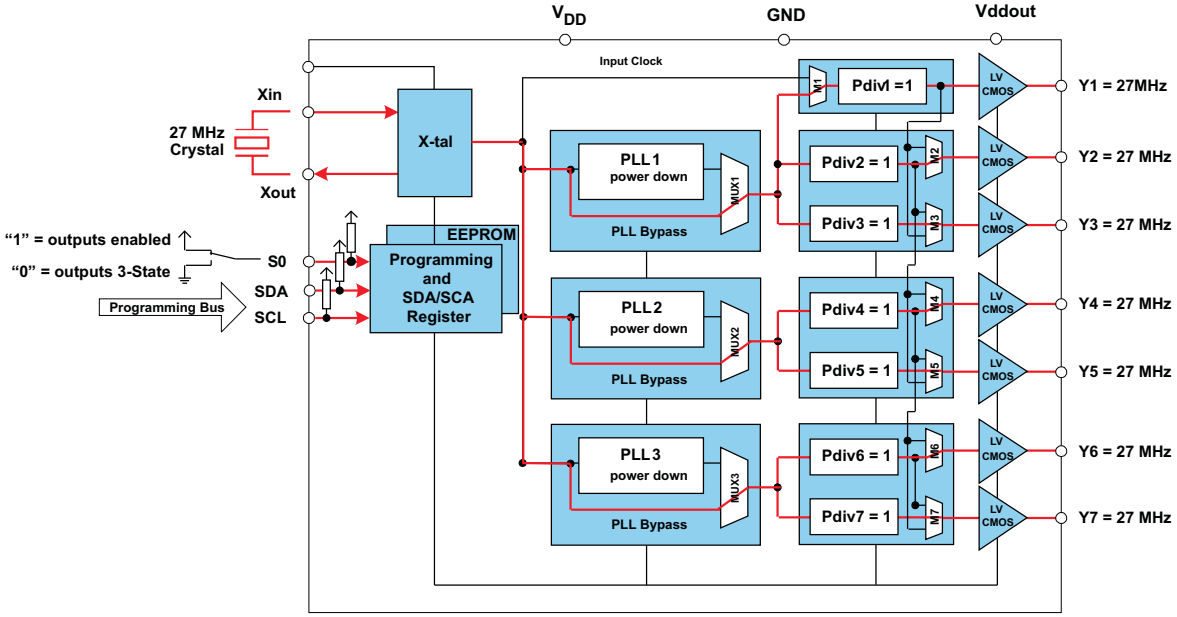


Figure 6. Default Device Setting

Table 4 shows the factory default setting for the Control Terminal Register (external control pins). In normal operation, all 8 register settings are available, but in the default configuration only the first two settings (0 and 1) can be selected with S0, as S1 and S2 configured as programming pins in default mode.

Table 4. Factory Default Setting for Control Terminal Register(1)

			Y1	PLL1 Settings			PLL2 Settings			PLL3 Settings		
External Control Pins			Output Selection	Frequency Selection	SSC Selection	Output Selection	Frequency Selection	SSC Selection	Output Selection	Frequency Selection	SSC Selection	Output Selection
S2	*S1*	**S0**	**Y1**	*FS1*	*SSC1*	**Y2Y3**	***FS2***	***SSC2***	**Y4Y5**	***FS3***	***SSC3***	**Y6Y7**
SCL (I2C)	SDA (I2C)	**0**	**3-state**	f_{VCO1_0}	off	**3-state**	f_{VCO2_0}	off	**3-state**	f_{VCO1_0}	off	**3-state**
SCL (I2C)	SDA (I2C)	**1**	**enabled**	f_{VCO1_0}	off	**enabled**	f_{VCO2_0}	off	**enabled**	f_{VCO1_0}	off	**enabled**

(1) In default mode or when programmed respectively, S1 and S2 act as serial programming interface, SDA/SCL. They do not have any control-pin function but they are internally interpreted as if S1=0 and S2=0. S0, however, is a control-pin which in the default mode switches all outputs ON or OFF (as previously predefined).

SDA/SCL SERIAL INTERFACE

The CDCE937/CDCEL937 operates as a slave device of the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I^2C specification. It operates in the standard-mode transfer (up to 100kbit/s) and fast-mode transfer (up to 400kbit/s) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDC9xx are dual function pins. In the default configuration they are used as SDA/SCL serial programming interface. They can be re-programmed as general purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, Byte 02, Bit [6].

DATA PROTOCOL

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of Bytes read-out are defined by Byte Count in the Generic Configuration Register. At Block Read instruction all bytes defined in the Byte Count has to be readout to correctly finish the read cycle.

Once a byte has been sent, it is written into the internal register and is effective immediately. This applies to each transferred byte independent of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM Write Cycle is initiated, the internal SDA register contents are written into the EEPROM. During this write cycle, data is not accepted at the SDA/SCL bus until the write cycle is completed. However, data can be read during the programming sequence (Byte Read or Block Read). The programming status can be monitored by reading *EEPIP*, Byte 01–Bit [6].

The offset of the indexed byte is encoded in the command code, as described in Table 5.

Table 5. Slave Receiver Address (7 Bits)

DEVICE	A6	A5	A4	A3	A2	A1(1)	A0(1)	R/$\overline{W}$
CDCE913/CDCEL913	1	1	0	0	1	0	1	1/0
CDCE925/CDCEL925	1	1	0	0	1	0	0	1/0
CDCE937/CDCEL937	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1/0**
CDCE949/CDCEL949	1	1	0	1	1	0	0	1/0

(1) Address bits A0 and A1 are programmable via the SDA/SCL bus (Byte 01, Bit [1:0]). This allows addressing up to 4 devices connected to the same SDA/SCL bus. The least-significant bit of the address byte designates a write or read operation.

COMMAND CODE DEFINITION

Table 6. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Byte Offset for *Byte Read*, *Block Read*, *Byte Write* and *Block Write* operation.

Generic Programming Sequence

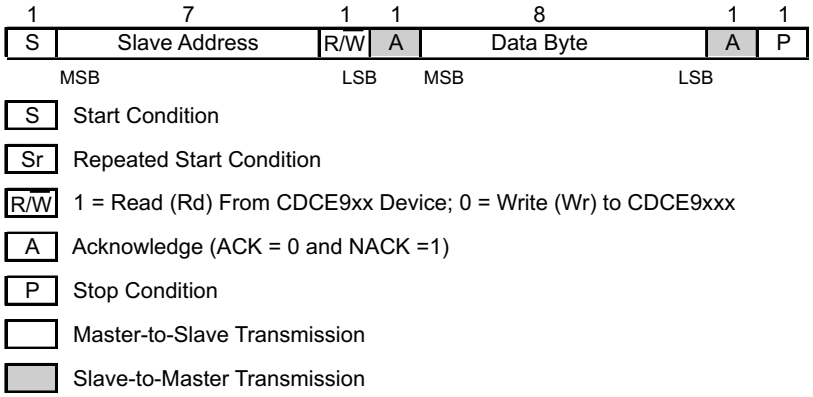


Figure 7. Generic Programming Sequence

Byte Write Programming Sequence

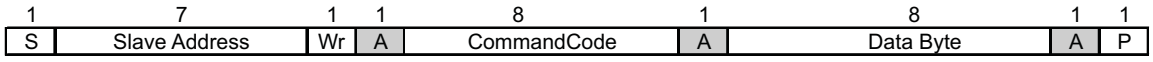


Figure 8. Byte Write Protocol

Byte Read Programming Sequence

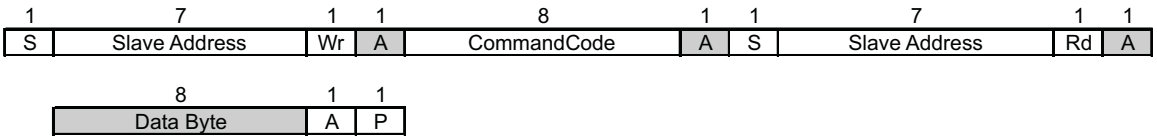
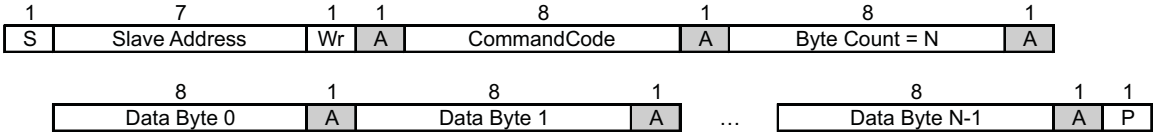


Figure 9. Byte Read Protocol

Block Write Programming Sequence



(1) Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, it is used for internal test purpose and should not be overwritten.

Figure 10. Block Write Protocol

Block Read Programming Sequence

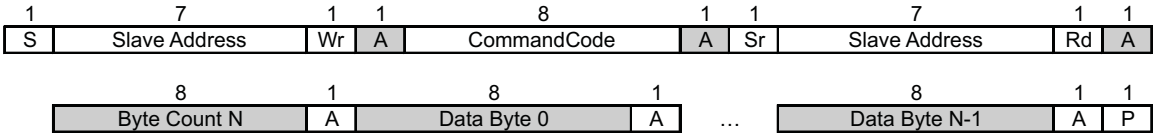


Figure 11. Block Read Protocol

Timing Diagram for the SDA/SCL Serial Control Interface

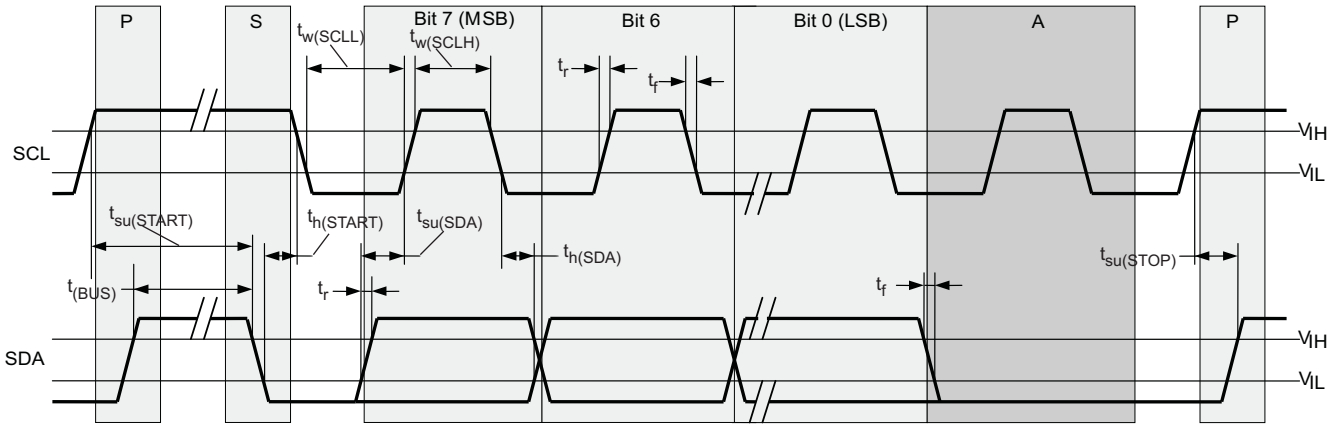


Figure 12. Timing Diagram for SDA/SCL Serial Control Interface

SDA/SCL HARDWARE INTERFACE

Figure 13 shows how the CDCE937/CDCEL937 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_P) depends on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 kΩ. It must meet the minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages (for more details see SMBus or I^2C Bus specification).

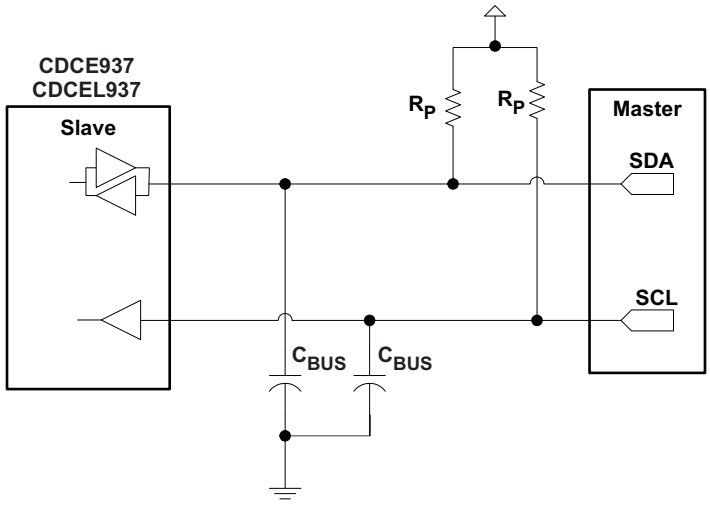


Figure 13. SDA / SCL Hardware Interface

SDA/SCL CONFIGURATION REGISTERS

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCE937/CDCEL937. All settings can be manually written into the device via the SDA/SCL bus or easily programmed by using the TI Pro-Clock™ software. TI Pro-Clock™ software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 7. SDA/SCL Registers

Address Offset	Register Description	Table
00h	Generic Configuration Register	Table 9
10h	PLL1 Configuration Register	Table 10
20h	PLL2 Configuration Register	Table 11
30h	PLL3 Configuration Register	Table 12

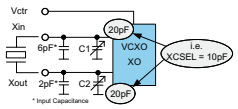
The grey-highlighted bits, described in the Configuration Registers tables in the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2 (see the *Control Terminal Configuration* section).

Table 8. Configuration Register, External Control Terminals

				Y1	PLL1 Settings			PLL2 Settings			PLL3 Settings		
	External Control Pins			Output Selection	Freq. Selection	SSC Selection	Output Selection	Freq. Selection	SSC Selection	Output Selection	Freq. Selection	SSC Selection	Output Selection
	S2	S1	S0	Y1	FS1	SSC1	Y2Y3	FS2	SSC2	Y4Y5	FS3	SSC3	Y6Y7
0	0	0	0	Y1_0	FS1_0	SSC1_0	Y2Y3_0	FS2_0	SSC2_0	Y4Y5_0	FS3_0	SSC3_0	Y6Y7_0
1	0	0	1	Y1_1	FS1_1	SSC1_1	Y2Y3_1	FS2_1	SSC2_1	Y4Y5_1	FS3_1	SSC3_1	Y6Y7_1
2	0	1	0	Y1_2	FS1_2	SSC1_2	Y2Y3_2	FS2_2	SSC2_2	Y4Y5_2	FS3_2	SSC3_2	Y6Y7_2
3	0	1	1	Y1_3	FS1_3	SSC1_3	Y2Y3_3	FS2_3	SSC2_3	Y4Y5_3	FS3_3	SSC3_3	Y6Y7_3
4	1	0	0	Y1_4	FS1_4	SSC1_4	Y2Y3_4	FS2_4	SSC2_4	Y4Y5_4	FS3_4	SSC3_4	Y6Y7_4
5	1	0	1	Y1_5	FS1_5	SSC1_5	Y2Y3_5	FS2_5	SSC2_5	Y4Y5_5	FS3_5	SSC3_5	Y6Y7_5
6	1	1	0	Y1_6	FS1_6	SSC1_6	Y2Y3_6	FS2_6	SSC2_6	Y4Y5_6	FS3_6	SSC3_6	Y6Y7_6
7	1	1	1	Y1_7	FS1_7	SSC1_7	Y2Y3_7	FS2_7	SSC2_7	Y4Y5_7	FS3_7	SSC3_7	Y6Y7_7
	Address Offset(1)			04h	13h	10h–12h	15h	23h	20h–22h	25h	33h	30h–32h	35h

(1) Address Offset refers to the byte address in the Configuration Register in the following pages.

Table 9. Generic Configuration Register

Offset[1]	Bit[2]	Acronym	Default[3]	Description
00h	7	E_EL	Xb	Device identification (read-only): 1 is CDCE937 (3.3 V), 0 is CDCEL937 (1.8 V)
	6:4	RID	Xb	Revision Identification Number (read only)
	3:0	VID	1h	Vendor Identification Number (read only)
01h	7	–	0b	Reserved – always write 0
	6	EEPIP	0b	EEPROM Programming Status:[4] (read only) 0 – EEPROM programming is completed 1 – EEPROM is in programming mode
	5	EELOCK	0b	Permanently Lock EEPROM Data[5] 0 – EEPROM is not locked 1 – EEPROM will be permanently locked
	4	PWDN	0b	Device Power Down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – device active (PLL1 and all outputs are enabled) 1 – device power down (PLL1 in power down and all outputs in 3-state)
	3:2	INCLK	00b	Input clock selection: 00 – Xtal 01 – VCXO 10 – LVCMOS 11 – reserved
	1:0	SLAVE_ADR	01b	Programmable Address Bits A0 and A1 of the Slave Receiver Address
02h	7	M1	1b	Clock source selection for output Y1: 0 – input clock 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pin 18/19[6] 0 – serial programming interface SDA (pin 19) and SCL (pin 18) 1 – control pins S1 (pin 19) and S2 (pin 18)
	5:4	Y1_ST1	11b	Y1-State0/1 Definition
	3:2	Y1_ST0	01b	00 – device power down (all PLLs in power down and all outputs in 3-State) 10 – Y1 disabled to low 01 – Y1 disabled to 3-state 11 – Y1 enabled
	1:0	Pdiv1 [9:8]	001h	10-Bit Y1-Output-Divider Pdiv1: 0 – divider reset and stand-by 1-to-1023 – divider value
03h	7:0	Pdiv1 [7:0]		
04h	7	Y1_7	0b	Y1_ST0/Y1_ST1 State Selection[7] 0 – State0 (predefined by Y1_ST0) 1 – State1 (predefined by Y1_ST1)
	6	Y1_6	0b	
	5	Y1_5	0b	
	4	Y1_4	0b	
	3	Y1_3	0b	
	2	Y1_2	0b	
	1	Y1_1	1b	
	0	Y1_0	0b	
05h	7:3	XCSEL	0Ah	Crystal Load Capacitor Selection[8] 00h → 0 pF 01h → 1 pF 02h → 2 pF : 14h-to-1Fh → 20 pF 
	2:0		0b	Reserved – do not write other than 0
06h	7:1	BCOUNT	40h	7-Bit Byte Count (defines the number of bytes which will be sent from this device at the next Block Read transfer); **all** bytes have to be read out to correctly finish the read cycle.)
	0	EEWRITE	0b	Initiate EEPROM Write Cycle[4] [9] 0– no EEPROM write cycle 1 – start EEPROM write cycle (internal configuration register is saved to the EEPROM)

(1) Writing data beyond '40h' may affect device function.
(2) All data transferred with the MSB first.
(3) Unless customer-specific setting.
(4) During EEPROM programming, no data is allowed to be sent to the device via the SDA/SCL bus until the programming sequence is completed. Data, however, can be read out during the programming sequence (Byte Read or Block Read).
(5) If this bit is set to high in the EEPROM, the actual data in the EEPROM will be permanently locked. There is no further programming possible. Data, however can still be written via SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only, if written into the EEPROM!
(6) Selection of "control pins" is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL), and the two slave receiver address bits are reset to A0="0" and A1="0".
(7) These are the bits of the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.
(8) The internal load capacitor (C1, C2) has to be used to achieve the best clock performance. External capacitors should be used only to finely adjust C_L by a few pF's. The value of C_L can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For C_L > 20 pF, use additional external capacitors. Also, the value of the device input capacitance has to be considered which always adds 1.5 pF (6 pF//2 pF) to the selected C_L. For more information about VCXO configuration and crystal recommendation, see application report SCAA085.
(9) Note: The EEPROM WRITE bit must be sent last. This ensures that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level high does not trigger an EEPROM WRITE cycle. The EEWRITE bit has to be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.

Table 9. Generic Configuration Register (continued)

Offset[1]	Bit[2]	Acronym	Default[3]	Description
07h-0Fh		—	0h	Unused address range

Table 10. PLL1 Configuration Register

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
10h	7:5	SSC1_7 [2:0]	000b	SSC1: PLL1 SSC Selection (Modulation Amount)[4] **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC1_6 [2:0]	000b	
	1:0	SSC1_5 [2:1]	000b	
11h	7	SSC1_5 [0]		
	6:4	SSC1_4 [2:0]	000b	
	3:1	SSC1_3 [2:0]	000b	
	0	SSC1_2 [2]	000b	
12h	7:6	SSC1_2 [1:0]		
	5:3	SSC1_1 [2:0]	000b	
	2:0	SSC1_0 [2:0]	000b	
13h	7	FS1_7	0b	FS1_x: PLL1 Frequency Selection[4] 0 – f_{VCO1_0} (predefined by PLL1_0 – Multiplier/Divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – Multiplier/Divider value)
	6	FS1_6	0b	
	5	FS1_5	0b	
	4	FS1_4	0b	
	3	FS1_3	0b	
	2	FS1_2	0b	
	1	FS1_1	0b	
	0	FS1_0	0b	
14h	7	MUX1	1b	PLL1 Multiplexer: 0 – PLL1 1 – PLL1 Bypass (PLL1 is in power down)
	6	M2	1b	Output Y2 Multiplexer: 0 – Pdiv1 1 – Pdiv2
	5:4	M3	10b	Output Y3 Multiplexer: 00 – Pdiv1-Divider 01 – Pdiv2-Divider 10 – Pdiv3-Divider 11 – reserved
	3:2	Y2Y3_ST1	11b	Y2, Y3-State0/1definition: 00 – Y2/Y3 disabled to 3-State (PLL1 is in power down) 01 – Y2/Y3 disabled to 3-State 10–Y2/Y3 disabled to low 11 – Y2/Y3 enabled
	1:0	Y2Y3_ST0	01b	
15h	7	Y2Y3_7	0b	Y2Y3_x Output State Selection[4] 0 – state0 (predefined by Y2Y3_ST0) 1 – state1 (predefined by Y2Y3_ST1)
	6	Y2Y3_6	0b	
	5	Y2Y3_5	0b	
	4	Y2Y3_4	0b	
	3	Y2Y3_3	0b	
	2	Y2Y3_2	0b	
	1	Y2Y3_1	1b	
	0	Y2Y3_0	0b	

(1) Writing data beyond 40h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 10. PLL1 Configuration Register (continued)

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
16h	7	SSC1DC	0b	PLL1 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv2	01h	7-Bit Y2-Output-Divider Pdiv2: 0 – reset and stand-by 1-to-127 is divider value
17h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv3	01h	7-Bit Y3-Output-Divider Pdiv3: 0 – reset and stand-by 1-to-127 is divider value
18h	7:0	PLL1_0N [11:4]	004h	PLL1_0[5]: 30-Bit Multiplier/Divider value for frequency f_{VCO1_0} (for more information, see paragraph *PLL Multiplier/Divider Definition*).
19h	7:4	PLL1_0N [3:0]		
	3:0	PLL1_0R [8:5]	000h	
1Ah	7:3	PLL1_0R[4:0]		
	2:0	PLL1_0Q [5:3]	10h	
1Bh	7:5	PLL1_0Q [2:0]		
	4:2	PLL1_0P [2:0]	010b	
	1:0	VCO1_0_RANGE	00b	f_{VCO1_0} range selection: 00 – f_{VCO1_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_0} < 175 MHz 11 – f_{VCO1_0} ≥ 175 MHz
1Ch	7:0	PLL1_1N [11:4]	004h	PLL1_1[5]: 30-Bit Multiplier/Divider value for frequency f_{VCO1_1} (for more information see paragraph *PLL Multiplier/Divider Definition*)
1Dh	7:4	PLL1_1N [3:0]		
	3:0	PLL1_1R [8:5]	000h	
1Eh	7:3	PLL1_1R[4:0]		
	2:0	PLL1_1Q [5:3]	10h	
1Fh	7:5	PLL1_1Q [2:0]		
	4:2	PLL1_1P [2:0]	010b	
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection: 00 – f_{VCO1_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_1} < 175 MHz 11 – f_{VCO1_1} ≥ 175 MHz

(5) PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511, 0<N<4096

Table 11. PLL2 Configuration Register

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
20h	7:5	SSC2_7 [2:0]	000b	SSC2: PLL2 SSC Selection (Modulation Amount)[4] **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC2_6 [2:0]	000b	
	1:0	SSC2_5 [2:1]	000b	
21h	7	SSC2_5 [0]		
	6:4	SSC2_4 [2:0]	000b	
	3:1	SSC2_3 [2:0]	000b	
	0	SSC2_2 [2]	000b	
22h	7:6	SSC2_2 [1:0]		
	5:3	SSC2_1 [2:0]	000b	
	2:0	SSC2_0 [2:0]	000b	
23h	7	FS2_7	0b	FS2_x: PLL2 Frequency Selection[4] 0 – f_{VCO2_0} (predefined by PLL2_0 – Multiplier/Divider value) 1 – f_{VCO2_1} (predefined by PLL2_1 – Multiplier/Divider value)
	6	FS2_6	0b	
	5	FS2_5	0b	
	4	FS2_4	0b	
	3	FS2_3	0b	
	2	FS2_2	0b	
	1	FS2_1	0b	
	0	FS2_0	0b	
24h	7	MUX2	1b	PLL2 Multiplexer: 0 – PLL2; 1 – PLL2 Bypass (PLL2 is in power down)
	6	M4	1b	Output Y4 Multiplexer: 0 – Pdiv2; 1 – Pdiv4
	5:4	M5	10b	Output Y5 Multiplexer: 00 – Pdiv2-Divider; 01 – Pdiv4-Divider; 10 – Pdiv5-Divider; 11 – reserved
	3:2	Y4Y5_ST1	11b	Y4, Y5-State0/1definition: 00 – Y4/Y5 disabled to 3-State (PLL2 is in power down); 01 – Y4/Y5 disabled to 3-State; 10–Y4/Y5 disabled to low; 11 – Y4/Y5 enabled
	1:0	Y4Y5_ST0	01b	
25h	7	Y4Y5_7	0b	Y4Y5_x Output State Selection[4] 0 – state0 (predefined by Y4Y5_ST0) 1 – state1 (predefined by Y4Y5_ST1)
	6	Y4Y5_6	0b	
	5	Y4Y5_5	0b	
	4	Y4Y5_4	0b	
	3	Y4Y5_3	0b	
	2	Y4Y5_2	0b	
	1	Y4Y5_1	1b	
	0	Y4Y5_0	0b	

(1) Writing data beyond 40h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 11. PLL2 Configuration Register (continued)

OFFSET(1)	Bit(2)	Acronym	Default(3)	DESCRIPTION
26h	7	SSC2DC	0b	PLL2 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv4	01h	7-Bit Y4-Output-Divider Pdiv4: 0 – reset and stand-by 1-to-127 – divider value
27h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv5	01h	7-Bit Y5-Output-Divider Pdiv5: 0 – reset and stand-by 1-to-127 – divider value
28h	7:0	PLL2_0N [11:4	004h	PLL2_0(5): 30-Bit Multiplier/Divider value for frequency f_{VCO2_0} (for more information see paragraph *PLL Multiplier/Divider Definition*)
29h	7:4	PLL2_0N [3:0]		
	3:0	PLL2_0R [8:5]	000h	
2Ah	7:3	PLL2_0R[4:0]		
	2:0	PLL2_0Q [5:3]	10h	
2Bh	7:5	PLL2_0Q [2:0]		
	4:2	PLL2_0P [2:0]	010b	
	1:0	VCO2_0_RANGE	00b	f_{VCO2_0} range selection: 00 – f_{VCO2_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO2_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO2_0} < 175 MHz 11 – f_{VCO2_0} ≥ 175 MHz
2Ch	7:0	PLL2_1N [11:4]	004h	PLL2_1(5): 30-Bit Multiplier/Divider value for frequency f_{VCO2_1} (for more information see paragraph *PLL Multiplier/Divider Definition*)
2Dh	7:4	PLL2_1N [3:0]		
	3:0	PLL2_1R [8:5]	000h	
2Eh	7:3	PLL2_1R[4:0]		
	2:0	PLL2_1Q [5:3]	10h	
2Fh	7:5	PLL2_1Q [2:0]		
	4:2	PLL2_1P [2:0]	010b	
	1:0	VCO2_1_RANGE	00b	f_{VCO2_1} range selection: 00 – f_{VCO2_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO2_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO2_1} < 175 MHz 11 – f_{VCO2_1} ≥ 175 MHz

(5) PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511, 0<N<4096

Table 12. PLL3 Configuration Register

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
30h	7:5	SSC3_7 [2:0]	000b	SSC3: PLL3 SSC Selection (Modulation Amount)[4] **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC3_6 [2:0]	000b	
	1:0	SSC3_5 [2:1]	000b	
31h	7	SSC3_5 [0]		
	6:4	SSC3_4 [2:0]	000b	
	3:1	SSC3_3 [2:0]	000b	
	0	SSC3_2 [2]	000b	
32h	7:6	SSC3_2 [1:0]		
	5:3	SSC3_1 [2:0]	000b	
	2:0	SSC3_0 [2:0]	000b	
33h	7	FS3_7	0b	FS3_x: PLL3 Frequency Selection[4] 0 – f_{VCO3_0} (predefined by PLL3_0 – Multiplier/Divider value) 1 – f_{VCO3_1} (predefined by PLL3_1 – Multiplier/Divider value)
	6	FS3_6	0b	
	5	FS3_5	0b	
	4	FS3_4	0b	
	3	FS3_3	0b	
	2	FS3_2	0b	
	1	FS3_1	0b	
	0	FS3_0	0b	
34h	7	MUX3	1b	PLL3 Multiplexer: 0 – PLL3 1 – PLL3 Bypass (PLL3 is in power down)
	6	M6	1b	Output Y6 Multiplexer: 0 – Pdiv4 1 – Pdiv6
	5:4	M7	10b	Output Y7 Multiplexer: 00 – Pdiv4-Divider 01 – Pdiv6-Divider 10 – Pdiv7-Divider 11 – reserved
	3:2	Y6Y7_ST1	11b	Y6, Y7-State0/1definition: 00 – Y6/Y7 disabled to 3-State and PLL3 power down 01 – Y6/Y7 disabled to 3-State 10 –Y6/Y7 disabled to low 11 – Y6/Y7 enabled
	1:0	Y6Y7_ST0	01b	
35h	7	Y6Y7_7	0b	Y6Y7_x Output State Selection[4] 0 – state0 (predefined by Y6Y7_ST0) 1 – state1 (predefined by Y6Y7_ST1)
	6	Y6Y7_6	0b	
	5	Y6Y7_5	0b	
	4	Y6Y7_4	0b	
	3	Y6Y7_3	0b	
	2	Y6Y7_2	0b	
	1	Y6Y7_1	1b	
	0	Y6Y7_0	0b	

(1) Writing data beyond 40h may affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) These are the bits of the *Control Terminal Register*. The user can pre-define up to eight different control settings. At normal device operation, these setting can be selected by the external control pins, S0, S1, and S2.

Table 12. PLL3 Configuration Register (continued)

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
36h	7	SSC3DC	0b	PLL3 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv6	01h	7-Bit Y6-Output-Divider Pdiv6: 0 – reset and stand-by 1-to-127 – divider value
37h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv7	01h	7-Bit Y7-Output-Divider Pdiv7: 0 – reset and stand-by 1-to-127 – divider value
38h	7:0	PLL3_0N [11:4]	004h	PLL3_0[5]: 30-Bit Multiplier/Divider value for frequency f_{VCO3_0} (for more information see paragraph *PLL Multiplier/Divider Definition*)
39h	7:4	PLL3_0N [3:0]		
	3:0	PLL3_0R [8:5]	000h	
3Ah	7:3	PLL3_0R[4:0]		
	2:0	PLL3_0Q [5:3]	10h	
3Bh	7:5	PLL3_0Q [2:0]		
	4:2	PLL3_0P [2:0]	010b	
	1:0	VCO3_0_RANGE	00b	f_{VCO3_0} range selection: 00 – f_{VCO3_0} < 125 MHz; 01 – 125 MHz ≤ f_{VCO3_0} < 150 MHz; 10 – 150 MHz ≤ f_{VCO3_0} < 175 MHz; 11 – f_{VCO3_0} ≥ 175 MHz
3Ch	7:0	PLL3_1N [11:4]	004h	PLL3_1[5]: 30-Bit Multiplier/Divider value for frequency f_{VCO3_1} (for more information see paragraph *PLL Multiplier/Divider Definition*)
3Dh	7:4	PLL3_1N [3:0]		
	3:0	PLL3_1R [8:5]	000h	
3Eh	7:3	PLL3_1R[4:0]		
	2:0	PLL3_1Q [5:3]	10h	
3Fh	7:5	PLL3_1Q [2:0]		
	4:2	PLL3_1P [2:0]	010b	
	1:0	VCO3_1_RANGE	00b	f_{VCO3_1} range selection: 00 – f_{VCO3_1} < 125 MHz; 01 – 125 MHz ≤ f_{VCO3_1} < 150 MHz; 10 – 150 MHz ≤ f_{VCO3_1} < 175 MHz; 11 – f_{VCO3_1} ≥ 175 MHz

(5) PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511, 0<N<4096

PLL Multiplier/Divider Definition

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCE937/CDCEL937 can be calculated:

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M} \quad (1)$$

where

M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL;
Pdiv (1 to 127) is the output divider.

The target VCO frequency (f_{VCO}) of each PLL can be calculated:

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

The PLL internally operates as fractional divider and needs the following multiplier/divider settings:

N

$P = 4 - \text{int}\left(\log_2 \frac{N}{M}\right)$ [if $P < 0$ then $P = 0$]

$Q = \text{int}\left(\frac{N'}{M}\right)$

$R = N' - M \times Q$

where

$N' = N \times 2^P$
$N \geq M$
100 MHz < f_{VCO} > 200 MHz
$16 \leq q \leq 63$
$0 \leq p \leq 7$
$0 \leq r \leq 511$

Example:

for f_{IN} = 27 MHz; M = 1; N = 4; Pdiv = 2;

→ f_{OUT} = 54 MHz
→ f_{VCO} = 108 MHz
→ P = 4 – int($\log_2$4) = 4 – 2 = 2
→ N′ = 4 × 2^2 = 16
→ Q = int(16) = 16
→ R = 16 – 16 = 0

for f_{IN} = 27 MHz; M = 2; N = 11; Pdiv = 2;

→ f_{OUT} = 74.25 MHz
→ f_{VCO} = 148.50 MHz
→ P = 4 – int($\log_2$5.5) = 4 – 2 = 2
→ N′ = 11 × 2^2 = 44
→ Q = int(22) = 22
→ R = 44 – 44 = 0

The values for P, Q, R, and N' is automatically calculated when using TI Pro-Clock™ software.

REVISION HISTORY

Changes from Original (August 2007) to Revision A **Page**

- Changed from the device status Product preview to Production. 1

Changes from Revision A (September 2007) to Revision B **Page**

- Changed Terminal Functions Table - the pin numbers to correpond with pin outs on the package 2
- Changed the PACKAGE THERMAL RESISTANCE table 4
- Changed Table 9 RID default From: 0h To: Xb 16
- Added note to PWDN description, Table 9 16

Changes from Revision B (December 2007) to Revision C **Page**

- Changed Table 9 - SLAVE_ADR default value From: 00b To: 01b 16

Changes from Revision C (January 2009) to Revision D **Page**

- Added Note 3: SDA and SCL can go up to 3.6V as stated in the *Recommended Operating Conditions* table 3

Changes from Revision D (September 2009) to Revision E **Page**

- Deleted sentence - A different default setting can be programmed on customer request. Contact Texas Instruments sales or marketing representative for more information. 11

Changes from Revision E (October 2009) to Revision F **Page**

- Added PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511, 0<N<4096 foot to PLL1, PLL2, and PLL3 Configure Register Table 18
- Added PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511 to PLL Multiplier/Divider Definition Section 23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCE937PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE937	Samples
CDCE937PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE937	Samples
CDCE937PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE937	Samples
CDCE937PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE937	Samples
CDCEL937PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCEL937	Samples
CDCEL937PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCEL937	Samples
CDCEL937PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCEL937	Samples
CDCEL937PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCEL937	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CDCE937, CDCEL937 :

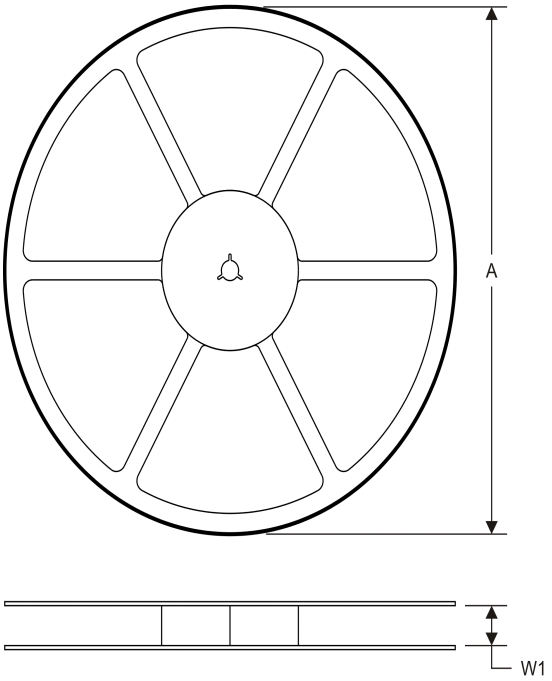
- Automotive: CDCE937-Q1, CDCEL937-Q1

NOTE: Qualified Version Definitions:

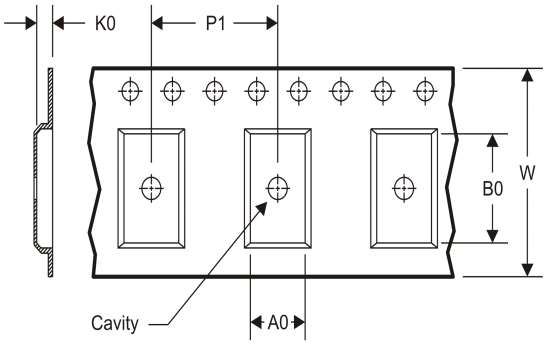
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



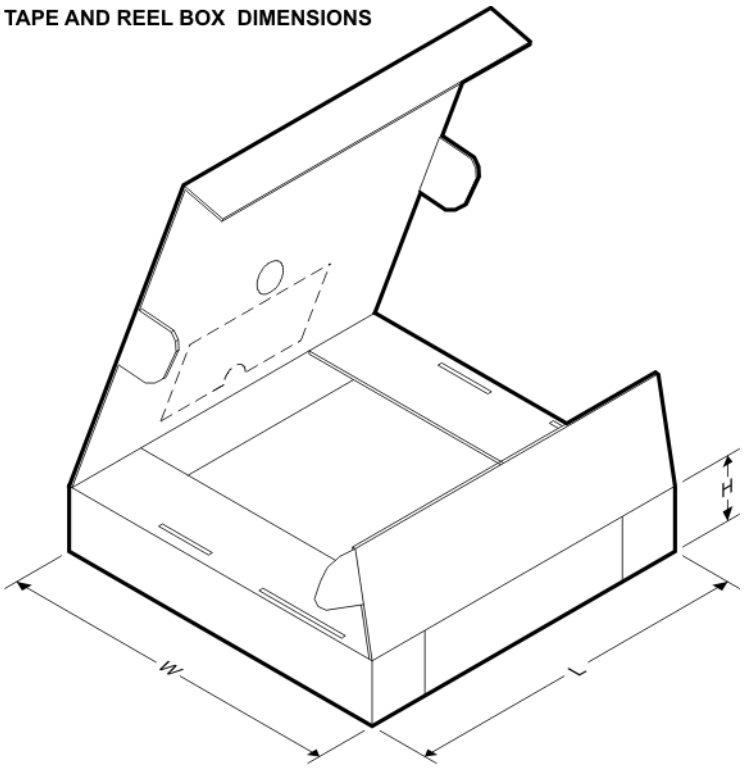
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE937PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CDCEL937PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

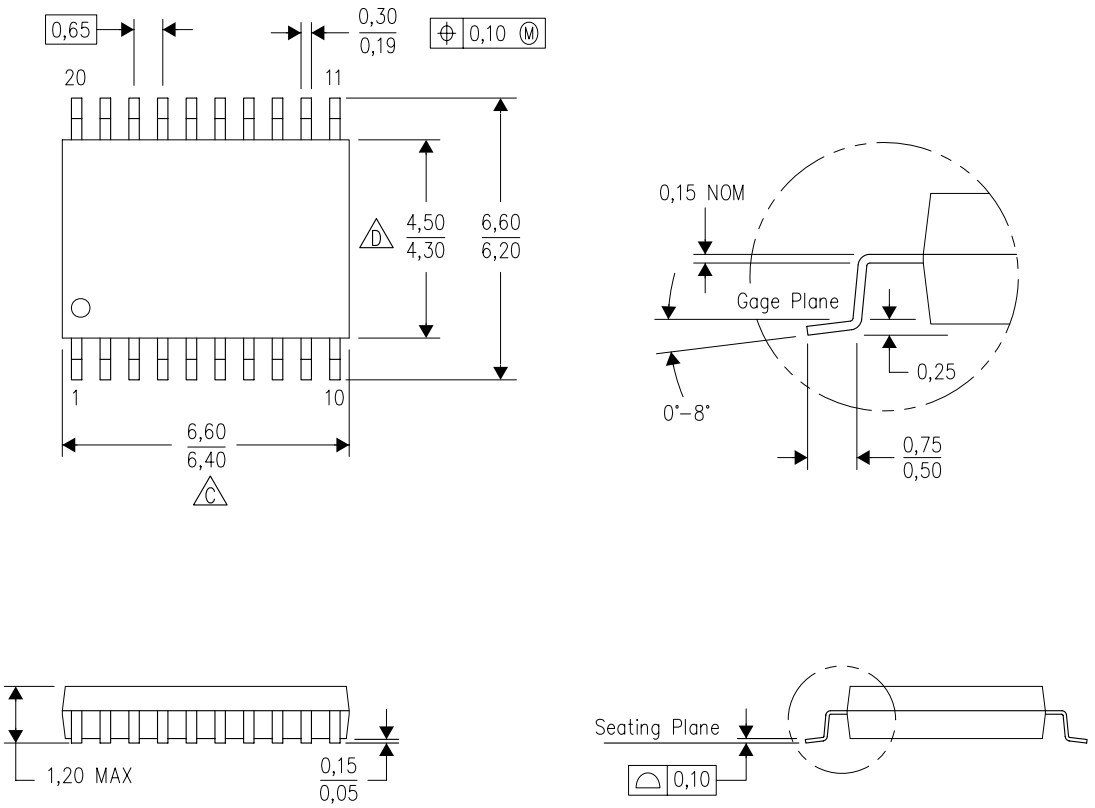
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE937PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
CDCEL937PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

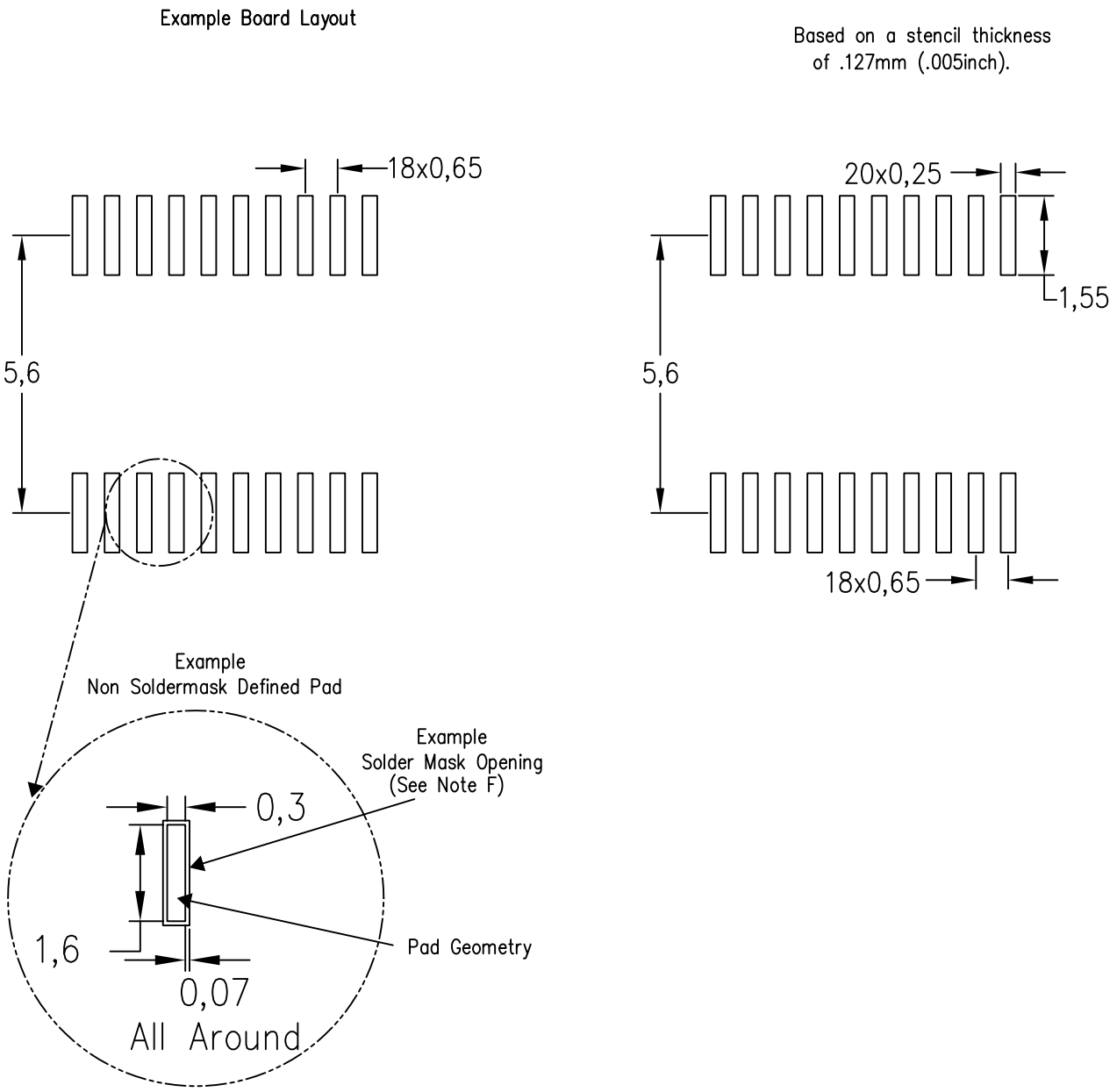
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265