OpenRISC Implementation in a ViaMask Structured ASIC

by Paul Dewell on 27-August-2004

1. Introduction

This article examines the use of the OpenRISC 1200 core implemented in a single-mask structured ASIC fabric. This example was originally developed and presented as a hands-on tutorial for the 2004 Design Automation Conference. We will outline the reasons for using the combination of an open core with a structured ASIC implementation, discuss the design flow used, and present the results of implementing this core in a structured ASIC architecture.

2. A Good Fit

The combination of open cores with structured ASICs provides a good fit for designers requiring low-cost, quick-turnaround solutions. The use of open cores decreases design costs compared to purchasing or developing IP. This choice can save a company on the order of $1,000,000. In a structured ASIC, a base set of photomasks are reused, so that only 1 to 8 masks need to be created for any design. A one-mask structured ASIC maximizes theses photomask savings, saving around $500,000 compared to a standard-cell implementation. Use of open cores can cut functional design and verification time in half. Similarly, structured ASICs typically provide faster flows for the physical design and can also cut several weeks off of IC manufacturing schedules.

3. The Design

For this design we chose the OpenRISC 1200 Microprocessor IP Core from the OpenRISC 1000 family at OpenCores.org. We used a 4K instruction size and data caches, and no QMEM (internal physical address space memory) or MMUs. This 32-bit scaler RISC uses approximately 600K transistors.

4. The Flow

The Synplicity Synplify tool was used to synthesize the RTL into a gate level netlist. For this run the default settings were used. This produced a 37,000 gate netlist for the functional logic without the RAM. The resulting runtime was about 2½ minutes on 1.8 GHz Opteron processor.

Next the gate level netlist was transformed using ViASIC's ViaPath tool into a logically equivalent netlist made from the 9 primitive components of the ViaMask structured ASIC library. The register files, instruction caches, and data caches were mapped into interleaved SRAM within the ViaMask architecture. The physical implementation used the TSMC 0.13 process version of the ViaMask library.

The physical design was created using ViaPath to perform memory generation, placement, and routing. All of the required routing connections were made through the instantiation of vias between metal3 and metal4 using the existing ViaMask routing-metal fabric. ViaPath was run using its default settings without scan insertion. The resulting runtimes for the physical design steps were 23 minutes from netlist to GDSII on a 1.8 GHz Opteron processor.

5. The Results.

Each logic tile of the ViaMask TSMC 0.13 library includes a 128 word by 32 bit dual-port SRAM and 256 logic cells (each logic cell containing 4 NAND2s, two MUX2s, a flip-flop and several programmable inverters). The various register files, instruction caches, and data caches required a total of 22 of the 128x32 SRAMS, using 22 logic tiles which provided 5,632 usable logic cells. ViaPath mapped the design into 3,208 logic cells so that this design turned out to be SRAM limited. This implementation required about 1.72mm2 of silicon area. Of this area, nine logic cells worth, or or about 41% of the logic gates, remained free for use. By adjusting the design to use 2K byte caches instead of 4K byte caches, the entire design could fit in 14 logic tiles taking about 1.1mm2 of silicon area. This implementation offers a reduction of 90% in silicon area compared to implementing this OpenRISC core in an FPGA.

6. Conclusion

The OpenRISC 1200 with 2K byte caches could be efficiently implemented in a 14 logic tile footprint of the ViASIC ViaMask TSMC 0.13 library. This provides about a 90% saving in die area with a similar piece price savings compared to an FPGA implementation. This open-core, structured-ASIC approach could save the designer around $1.5 million in costs and months in time-to-parts compared to a typical standard-cell implementation.

Additional information on the benefits on using structured ASICs and the specification of the available single-mask ViaMask libraries can be found on the ViASIC web site at www.viasic.com.

Additional information on available open cores including the OpenRISC 1200 can be found at www.opencores.org