Rois24_24uP instruction list

James C Brakefield 2016

Two read port and one write port LUT RAM; Single or dual port Block RAM

27 instructions, four formats

Categorey	format	nemonic (bold if coded)	hex opcode	binary opcode	phase	state	# phases	next inst	PC chg	LUT mem in	LUT adr	instruction summary	Block RAM data in	Block RAM adr	Blk RAM we	# test cases	comments
Call	DRS	CALL	32	110010		N		M(R+S)	Y	PC+1	D	R+S=>PC, PC+1=>D					
	DRN	CALLsN	36	011110		N		M(R+sN)	Y	PC+1	D	R+sN=>PC, PC+1=>D					
	DNN	CALLR	08	001000		N		M(PC+sNN)	Y	PC+1	D	PC+sNN=>PC, PC+1=>D					
	CRN	JMPCC	33	110011		N		R+S or PC+1	Y			if CC true R+S else PC+1 =>PC					
	CRN	**JMPCCsN**	**37**	**011111**		**N**		**R+sN or PC+1**	**Y**			**if CC true R+sN else PC+1 =>PC**					
	CNN	BRCC	09	001001		N		PC+sNN or PC+1	Y			if CC true PC+sNN else PC+1 =>PC					
LD/ST	DRS	LD	30	110000			2			M out	D	M(R+S)=>D					
		LD	30		1	N		no change to PC						R+S			generate block RAM adr
		LD	30		2	LD		PC+1		M out	D			PC+1			BRAM out into D, fetch next
	DRN	LDsN	11	010001		N	2	PC+1		M out	D	M(R+sN)=>D		R+sN			
	DNN	LDI	0A	001010		N		PC+1		sNN	D	sNN=>D					sign extended sNN=>D
	NNN	PFXsN	0B	001011		N		PC+1				sNNN=>PFX					18bit imm to prefix register
	DRS	ST	31	110001			2	PC+1				D=>M(R+S)	D	R+S	Y		
			31		1	N		no change to PC			D			R+S	Y		generate block RAM adr
			31		2	ST		PC+1						PC+1			fetch next inst
	DRN	STsN	13	010011		N	2	PC+1				D=>M(R+sN)	D	R+sN	Y		
	DRN	IN	18	011100		N		PC+1		IO in	D	IO(R+sN)=>D					
	DRN	**OUT**	**19**	**011101**		**N**		**PC+1**				**D=>IO(R+sN)**					
ALU	DRS	ADD	20	100000		N		PC+1		R+S	D	R+S=>D					
	DRN	**ADI**	**10**	**010000**		**N**		**PC+1**		**R+sN**	**D**	**R+sN=>D**					
	DRS	SUB	21	100001		N		PC+1		R-S	D	R-S=>D					
	DRS	ADC	22	100010		N		PC+1		R+S+cy	D	R+S+carry=>D					
	DRN	**ADCI**	**12**	**010010**		**N**		**PC+1**		**R+sN+cy**	**D**	**R+sN+carry=>D**					
	DRS	SBC	23	100011		N		PC+1		R-S+cy	D	R-S+carry=>D					
	DRS	AND	24	100100		N		PC+1		R&S	D	R&S=>D					
	DRN	ANDI	14	010100		N		PC+1		R&sN	D	R&sN=>D					
	DRS	ANDC	25	100101		N		PC+1		R&~S	D	R&~S=>D					
	DRS	OR	26	100110		N		PC+1		R|S	D	R|S=>D					
	DRN	ORI	16	010110		N		PC+1		R|sN	D	R|sN=>D					
	DRS	XOR	27	100111		N		PC+1		R^S	D	R^S=>D					
	DRN	XORI	17	010111		N		PC+1		R^~S	D	R^sN=>D					

Location 0 of register file always reads as zero (block any writes to D=0)

If sN and prefix reg loaded, PFX&sN=>sNNNN

PC limited to 16-bits, CC saved in upper 8-bits of return address

CCR: carry, overflow, MSB, exp all 1s, exp all 0s, mant all 1s, mant all 0s, LSB

```
DRS XXXXXX DDDDDD RRRRRR SSSSSS
NNN XXXXXX sNNNNN NNNNNN NNNNNN
CRN XXXXXX CCCCCC RRRRRR sNNNNN
DNN XXXXXX DDDDDD sNNNNN NNNNNN
CNN XXXXXX CCCCCC sNNNNN NNNNNN
```