TUTORIAL TEST SUIT SPACEWIRE

LATIN AMERICAN GROUP INTEGRATED CIRCUITS

GLADIC

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WHAT THIS PROJECT WISH HELP YOU

- Don't make you lose your head when you try run this
- Explain in basic way how to use this
- Make tests with a SystemC model Spacewire
- A test suit using graphical interface

OS type: Linux based rpm distro

Graphical Interface: GTK/GTKMM (minimal 2.16)

Compiler: g++/iverilog

API: boost,systemC,gtkm,gtkmm,glade

Obs: Need take a look on the flags during compilation to make sure are you compiling and link correctly with shared library. SystemC need to be compiled in separate and need to exported in order to code see systemC shared objects like icarus verilog vpi source code.

GRAPHICAL INTERFACE

GLADIC SPAC	EWIRE TEST TO	OL	
Auto Start	🗌 Link D	Disable	Set Flag
🗌 Eep Test	Time Co	ode Test	Start Test
Send Data		Enable Time Code	
ncy		Set	Frequency
Link Enable Au	to Start	Reset	Finish Simulation
	Auto Start Eep Test Send Data	Auto Start Link D Eep Test Time Co Send Data	Eep Test Time Code Test Send Data Enable Time Code

TEST SUIT SYSTEMC / VERILOG

erilog Test Suit				
		—	-	
Link Enable	Auto Start	Link	Disable	Set Flag
Test Suit Gladic				
Eop Test	🗌 Eep Test	🔲 Time 🤅	Code Test	Start Test
	Send Data		Enable Time Code	e
Frequency SystemC Enter Frequen				e t Frequency
Enter Frequen		Auto Start		

TEST SUIT SYSTEMC / VERILOG

1# This part consist in set pins of verilog side environment. In another words you have control by buttons. This aim validation to make specific case in order to check errors or validation where you can proof in time simulation the correct work of verilog/systemverilog hardware develop.

2# Now the part of environment. This contain the control over all simulation. You can change frequency rate from , reset entire system, generate data, time codes.

TEST SUIT FINISH SIMULATION

	GLADIC SE	PACEWIRE TEST T	OOL		×
Verilog Test Suit					_
Verilog Interface					
Link Enable	Auto Start	Link	k Disable	Set Flag	
Test Suit Gladic					
Eop Test	🗌 Eep Test	🔲 Time	Code Test	Start Test	
SysytemC Test Suit Tx Data SystemC	Send Data		Enable Time C	ode	
Frequency SystemC					
Enter Frequen	cy			Set Frequency	
Space Wire SystemC					_
Link Disable	Link Enable	Auto Start	Reset	Finish Simulation	
					_

3# This button finish simulation of environment systemC and verilog setting a variable on verilog to finish simulation and quit from icarus verilog simulator.

TEST SUIT RESET

	GLADIC SPAC	EWIRE TEST TOOL	
Verilog Test Suit			
Verilog Interface			
Link Enable	Auto Start	Link Disable	Set Flag
Test Suit Gladic			
Eop Test	🔲 Eep Test	Time Code Test	Start Test
	Sand Data	Enable Time C	ada
	Send Data	Enable Time C	ode
Frequency SystemC	Send Data	Enable Time C	ode
			ode Set Frequency
Frequency SystemC			
Frequency SystemC Enter Frequence Space Wire SystemC	y		

4# This button reset all the environment. When environment is executed by the first time you need reset both model and rtl SpaceWires. Not resetting you can expecting wrong behavior and crash execution.

TEST SUIT SYSTEMC AUTOSTART

	GLADIC SPACEWIRE TEST TOOL			
/erilog Test Suit				
Verilog Interface				
Link Enable	Auto Start	Link Disable	Set Flag	
Test Suit Gladic				
Eop Test	🔲 Eep Test	Time Code Test	Start Test	
Frequency SystemC	Send Data	Enable Time Co	ode	
Enter Frequenc	у		Set Frequency	
Space Wire SystemC				
Link Disable	Link Enable Aut	to Start Reset	Finish Simulation	
		5#		

5# This button is present on specification on the SystemC model. In the way to we use it like a spacewire AutoStart wait another Spacewire to start communicate to start send NULL's" ECSS-E-ST-50-12C(31July2008)". Before first reset Auto Start is not enabled.

TEST SUIT SYSTEMC LINKENABLE

	GLADIC SPAC	EWIRE TEST TOOL		
Verilog Test Suit				
Verilog Interface				
Link Enable	Auto Start	Link Disabl	e	Set Flag
Test Suit Gladic				
Eop Test	🔲 Eep Test	Time Code T	est	Start Test
Tx Data SystemC Frequency SystemC	Send Data	Enat	le Time Code	
Enter Frequenc	У		Set	Frequency
Space Wire SystemC				
	Link Enable Aut	to Start	Reset	Finish Simulation
Link Disable				

6# This button is present on specification on the SystemC model. In the way to we use it like a spacewire Linkenable initialize the line sending NULLs to another Spacewire to start communicate and send NULL's "ECSS-E-ST-50-12C(31July2008)". Before first reset LinkEnable is not enabled.

TEST SUIT LINKDISABLE

	GLADIC SPAC	EWIRE TEST TO	OL	
/erilog Test Suit				
Verilog Interface				
Link Enable	Auto Start	Link [Disable	Set Flag
Test Suit Gladic				
Eop Test	📃 Eep Test	🔲 Time C	ode Test	Start Test
Frequency SystemC	Send Data		Enable Time Code	
Enter Frequenc	У		Set	: Frequency
Space Wire SystemC				
	Link Enable Au	uto Start	Reset	Finish Simulation
Link Disable	LINK ENADLE	aco beare		

7# This button is present on specification on the SystemC model. This button disable spacewire according with definitions ECSS-E-ST-50-12C(31July2008). So when are you trying connect or on state run and this button is set the model will disconnect Before first reset LinkDisable is not enabled.

TEST SUIT FREQUENCY TX MODEL

	GLADIC SPA	CEWIRE TEST TO	OL	
/erilog Test Suit				
Verilog Interface				
Link Enable	Auto Start	Link [Disable	Set Flag
Test Suit Gladic				
🔲 Eop Test	🔲 Eep Test	🔲 Time C	ode Test	Start Test
SysytemC Test Suit				
Tx Data SystemC				
	Send Data		Enable Time Code	e
Frequency SystemC				
Enter Frequen	cy 🗌		Se	t Frequency
				8#
Space Wire SystemC				011
Link Disable	Link Enable A	uto Start	Reset	Finish Simulation
LINK Disable				

8# This give the chance to set frequency on TX spacewire in order to test. The valid frequencies are : 2 - 10 - 20 - 50 - 100 - 150 - 200 - 201 - 250 - 280. After the first reset TX model start at clock operation 10 MHz "May be changed during connection". Can change during data transfers/timecodes to check any problem in change frequency on RX verilog.

TEST SUIT DATA TX SEND

	GLADIC SPACEWIRE TEST TOOL				
/erilog Test Suit					
Verilog Interface					
Link Enable	Auto Start	Link Disable	Set Flag		
Test Suit Gladic					
📄 Eop Test	📃 Eep Test	Time Code Test	Start Test		
	Send Data	Enable Time Co	de		
SysytemC Test Suit Tx Data SystemC Frequency SystemC	Send Data	Enable Time Co	de		
Tx Data SystemC	9#		de Set Frequency		
Tx Data SystemC	9#				

9# You can send data from model to verilog. This generate a htm log. To get a better understand this button can be used only after you send data from verilog to systemc. It crash if you try without generate to verilog first.

TEST SUIT TIMECODE TX SEND

	GLADIC SPAC	CEWIRE TEST TOOL	
Verilog Test Suit			
Verilog Interface			
Link Enable	Auto Start	Link Disable	Set Flag
Test Suit Gladic			
🔲 Eop Test	🔲 Eep Test	Time Code Test	Start Test
Tx Data SystemC	Send Data	Enable Time Co 10#	ode
SysytemC Test Suit Tx Data SystemC Frequency SystemC Enter Freque		10#	
Tx Data SystemC		10#	ode Set Frequency

10# Time code is generated automatic when you hit the button. After and before reset timecode is disabled.

TEST SUIT N-CHAR TX SEND TEST

	GLADIC SPACEWIRE TEST TOOL				
erilog Test Suit					
/erilog Interface					
Link Enable	Auto Start	🗌 Link 🛛	Disable	Set Flag	
Test Suit Gladic					
🗌 Eop Test	📃 Eep Test	🗌 Time C	ode Test	Start Test	11#
	Send Data		Enable Time Code		
Tx Data SystemC	Send Data		Enable Time Code		
Tx Data SystemC				Frequency	
SysytemC Test Suit Tx Data SystemC Frequency SystemC Enter Freq Space Wire SystemC					

11# The Nchar test consist on build a package EOP - DATA - EOP ; EOP – DATA - EEP – EOP ; EOP – DATA/EEP/TIMECODE – EOP. EOP have high priority against EEP; time code can be executed in same time EOP/EEP tests.

TEST SUIT VERILOG PINS INTERFACE

	GLADIC SPACEWIRE TEST TOOL				
erilog Test Suit					
Link Enable	e 🗌 Auto Start	🗌 Link	Disable	Set Flag	12
Test Suit Gladic					
🔲 Eop Test	📃 Eep Test	🔲 Time 🤇	Code Test	Start Test	
Frequency SystemC	Send Data		Enable Time Cod	e	
Frequency SystemC					
Enter Free	quency		Se	t Frequency	
Space Wire SystemC					
	Link Enable	Auto Start	Reset	Finish Sim	ulation

12# This obey in the same way like described using SystemC." ECSS-E-ST-50-12C(31July2008)".

TEST SUIT OBSERVATIONS

- Still under development "issues about errors and data time between spacewires "
- We hope have some feedback"Help us and we help you"
- Donations are welcome !!!!! "nobody can survive eating systemc/systemverilog everyday" :-D
- Design is reluctant a bit cause bad code, but I hope he post soon as possible his solution "systemverilog"
- The environment is running on 500 MHz clock to be possible simulate SystemC/SysTemVerilog over 200 MHz
- There is two files on html where contain data comparison and what arrive from the line both sides
- If you have a question about configuration of environment enter in contact by github \rightarrow issues