

1.1

# **Tutorial for "ChipScope Pro"**



The Xilinx Tool "ChipScope Pro" facilitates the implementation of a Logic Analyser Core on the Spartan III board.

#### **Creation of a Logic Analyser Core** A "Core" file ~.cdc can be created with $\rightarrow$ **Project** $\rightarrow$ **New Source**. The following menu appears: X B BMM File Structure ChipScope Definition and Connection Embedded Processor File Name Implementation Constraints File 💐 IP (CoreGen & Architecture Wizard) ila\_spartan3 MEM File Location: 🚺 Schematic 🖹 State Diagram D:\ISEwork\BB1\b1 .... Test Bench Waveform 📄 User Document 🗹 Verilog Module 🔟 Verilog Test Fixture C VHDL Library 🗹 VHDL Module > Add to project Next > Cancel Help Picture 1: New Source Choose "ChipScope Definition and Connection", give a file name and activate the "Add to Project" option. Click "Next" to go on to the next menu: Source File Project Na Source Type: ChipScope Definition and Connection File Source Name: ila\_spartan3.cdc add1 Source Directory: D:\ISEwork\BB1\b1 < Back Next > Cancel < Back Finish Cancel Help

Picture 2: Assign to the top entity.

Choose the name of the top entity and click "Finish".

Picture 3: Summary

ce with th

Help

This way the "Core" file *ila\_spartan3.cdc* is included in the project.

Sources in Project:
Em 3 XC38400-5tq144
□····································
add1-bebaviour ( \adder1 vbd)
Picture 1: Included file ila_spartan3.cdc

#### 1.2 Usage of the system clock as LA clock

In order for the system clock to be available to the "ChipScope" Logic Analyser, the entity must be listed under ports in the VHDL source code:

SYSCLK : in bit; N\_SYSCLK : out bit; In the architecture, for instance: N\_SYSCLK <= not (SYSCLK); In the ~.ucf file: NET SYSCLK LOC = P127; NET N\_SYSCLK LOC = P46;

If a higher frequency is desired as circuit timing, a frequency increase up to approx. 400 MHz can be reached by using the DCM-module. For details see Appendix A.

### 1.3 Adaptation with "Core Inserter"

By double-clicking on the symbol of the ~.cdc file **\*** ila\_spartan3.cdc, the "Core Inserter" is invoked and 4 menus appear:

First menu: The netlist paths for input and output and the output directory

are specified. The device family is set to "SPARTAN 3".

The options: Use SRL 16s (SeriellShift LUT 16 bit) and RPMs (relationally placed macros) should be activated.

E DEVICE	DEVICE Select Device Options					
	Design Files					
	Input Design Netlist:	d:\isework\bb1\b1\add8_cs.ngc	Browse			
	Output Design Netlist:	d.\isework\bb1\b1\add8_cs.ngc	Browse			
	Output Directory:	d:\isework\bb1\b1\_ngo	Browse			
	Device Settings Device Family: Spart	an3 🗸				
	Device Settings Device Family: Spart	an3 v				

Picture 2: Menu 1

Second menu:

Disable JTAG Clock BUFG Insertion can remain inactive .

DEVICE	ICON	Select Integrated Controller Options
<b>ICON</b>	Parameters	
	< <u>Previous</u> Ne <u>x</u> t >	New ILA Unit New ATC2 Unit

Picture 3: Menu 2 Third menu: The trigger par

The trigger parameters are listed according to data length and allocation.

	are not neede	d for simple applications.
		ILA Select Integrated Logic Analyzer Options
		Trigger Parameters Capture Parameters Net Connections
	UU: ILA	Trigger Input and Match Unit Settings
		Number of Input Trigger Ports: 1 💌 Number of Match Units Used: 1
		TRIGO:
		Counter Width: Disabled V Functions: =, >
		Trigger Condition Settings
		Enable Trigger Sequencer Max Number of Sequencer Levels: 16
		Storage Qualification Condition Settings
		Enable Storage Qualification
		< Previous Next > Remove Unit
	Picture 4: Menu 3	3
Fourth menu:	Data registrati	ion parameters such as memory depth and data width of the
	trigger data an	nd clock edge are specified here.
		ILA Select Integrated Logic Analyzer Options
		Trigger Parameters Canture Parameters Net Connections
	······UU: ILA	Capture Settings
		Data Depth: 512 💌 Samples Sample On Rising 💌 Clock Edge
		V Data Same As Trigger
		-Trigger Date Lload is Date
		Ingger Folis Osed As Data Ingger Folis Osed
		Resource Utilization
		BlockRAMs used: 1
		<pre></pre>
E.01	Picture 5: Menu 4	
Fifth menu:	Under "Modif	ty Connections", the signals in the list must be assigned.
		ILA Select Integrated Logic Analyzer Options
	UO: ILA	Trigger Parameters Capture Parameters Net Connections
		Net Connections
		← TRIGGER PORTS
		Modify Connections
		< Previous Return to Project Navigator Remove Unit
	Picture 6: Menu 5	5
	The desired si	gnal is marked in the left side table, and the channel number on the right s
	click on "Mak	te Connections".

Trigger counters, trigger sequencer and storage qualification are not needed for simple applications.

Structure / Nets				Ne	et Selections	
—/ [add8]					Clock Signals	Trigger/Data Signals
•			►		hannel	
Net Name	Pattern:		▼ Filter		H:0 /SYSCLK_	IBUF
Net Name	Source Instance	Source Component	Base Type			
RC<2>	INST_2/COUT1	LUT3	LUT3		CPO	
RC<0>	INST_0/COUT1	LUT3	LUT3		010	
N_SYSCLK_OBUF	N_SYSCLK1_INV_0	INV	INV.			
SYSCLK_IBUF	SYSCLK_IBUF	IBUF	IBUF		Make Connections	1 Move Nets Up
CIN_IBUF	CIN_IBUF	IBUF	IBUF			
	1	l		- I F	Remove Connection:	s 🛛 🔶 Move Nets Down

Picture7: Menu 5.1 Modify Connections: Clock Signals

By clicking on "Net Name", the list of signal names is sorted alphabetically; a larger set of signals can be marked in the "Trigger Data Signals" list.

Structure / Nets					Ne	t Sele	ections	
—/ [add8]				-		lock	Signals	Trigger/Data Signal
					Cł	nanne	el .	
					CH	H:0	/SUM_0	_OBUF
					CH	1:1	/SUM_1	_obuf
					CH	1:2	SUM_2	_obuf
					CH	1:3	/SUM_3	_obuf
					СН	:4	/SUM_4_	_obuf
					СН	1:5	/SUM_5	_obuf
					СН	:6	/SUM_6	_OBUF
					CH	:/	SUM_7	_OROF
					CH	18	SUM_8	_UBUF
4						1.9 1-40	A_U_IBU	л <sup>.</sup>
•						.10	CIN_IBU	
Net Name	Pattern:		-	Filter	1			
Net Name	Source Instance	Source Component	Base Type					
RC<0>	INST OCOUT1	LUT3	11172					
	IN31_0/COOT1	2010	1013	-				
RC<1>	INST_1/COUT1	LUT3	LUT3	-				
RC<1> RC<2>	INST_1/COUT1 INST_2/COUT1	LUT3 LUT3	LUT3 LUT3					
RC<1> RC<2> RC<3>	INST_1/COUT1 INST_2/COUT1 INST_3/COUT1	LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3	_				
RC<1> RC<2> RC<3> RC<4>	INST_1/COUT1 INST_2/COUT1 INST_2/COUT1 INST_3/COUT1 INST_4/COUT1	LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3					
RC<1> RC<2> RC<2> RC<3> RC<4> RC<4>	INST_3/COUT1 INST_2/COUT1 INST_2/COUT1 INST_3/COUT1 INST_4/COUT1 INST_5/COUT1	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3					
RC<1> RC<2> RC<3> RC<4> RC<4> RC<5> RC<6>	INST_2/COUT1 INST_2/COUT1 INST_2/COUT1 INST_3/COUT1 INST_4/COUT1 INST_5/COUT1 INST_6/COUT1	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3					
RC<1> RC<2> RC<2> RC<3> RC<4> RC<5> RC<5> SUM_0_OBUF SUM_0_OBUF	INST_JACOUTI INST_JACOUTI INST_JACOUTI INST_JACOUTI INST_JACOUTI INST_JACOUTI INST_JAMSor_SI_Resu.	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3					
RC<1> RC<2> RC<2> RC<3> RC<4> RC<5> RC<5> SUM_0_OBUF SUM_1_OBUF SUM_1_OBUF	INST_1/COUT1 INST_2/COUT1 INST_3/COUT1 INST_3/COUT1 INST_5/COUT1 INST_5/COUT1 INST_5/COUT1 INST_6/COUT1 INST_0/Mxor_SI_Resu INST_1/Mxor_SI_Resu	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3					
RC<1> RC<2> RC<3> RC<3> RC<5> RC<5> SUM_0_0BUF SUM_1_0BUF SUM_2_0BUF SUM_2_0BUF	INST_ICOUTI INST_ICOUTI INST_2/COUTI INST_3/COUTI INST_3/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_1/Mxor_SI_Resu. INST_1/Mxor_SI_Resu.	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3					
RC<1> RC<2> RC<3> RC<4> RC<5> SUM_0_0BUF SUM_1_0BUF SUM_2_0BUF SUM_2_0BUF SUM_2_0BUF	INST_IACOUTI INST_IACOUTI INST_3/COUTI INST_3/COUTI INST_5/COUTI INST_5/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_2/Mxor_SI_Resu. INST_3/Mxor_SI_Resu.	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3					
RC<1> RC<2> RC<3> RC<44 RC<5> RC<6> SUM_0_0BUF SUM_2_0BUF SUM_3_0BUF SUM_4_0BUF SUM_4_0BUF	INST_IACOUTI INST_IACOUTI INST_2/COUTI INST_3/COUTI INST_4/COUTI INST_6/COUTI INST_0/Mxor_SI_Resu INST_0/Mxor_SI_Resu INST_3/Mxor_SI_Resu INST_4/Mxor_SI_Resu INST_4/Mxor_SI_Resu	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3			PO		
RC<1> RC<2> RC<3> RC<4> RC<4> RC<4> SUM_0_OBUF SUM_1_OBUF SUM_2_OBUF SUM_3_OBUF SUM_4_OBUF SUM_4_OBUF	INST_1/COUT1 INST_1/COUT1 INST_2/COUT1 INST_3/COUT1 INST_4/COUT1 INST_6/COUT1 INST_6/COUT1 INST_0/Mxor_SI_Resu. INST_0/Mxor_SI_Resu. INST_3/Mxor_SI_Resu. INST_4/Mxor_SI_Resu. INST_5/Mxor_SI_Resu.	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3			PO		
RC<1> RC<2> RC<3> RC<4> RC<5> RC<5> SUM_1_OBUF SUM_2_OBUF SUM_3_OBUF SUM_4_OBUF SUM_5_OBUF SUM_5_OBUF SUM_5_OBUF	INST_IACOUTI INST_IACOUTI INST_2/COUTI INST_3/COUTI INST_3/COUTI INST_5/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_6/Mxor_SI_Resu. INST_2/Mxor_SI_Resu. INST_5/Mxor_SI_Resu. INST_6/Mxor_SI_Resu.	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3			PO		
RC<1> RC<2> RC<3> RC<4> RC<5> RC=6 SUM_1_OBUF SUM_2_OBUF SUM_2_OBUF SUM_4_OBUF SUM_5_OBUF SUM_5_OBUF SUM_7_OBUF	INST_IACOUTI INST_IACOUTI INST_2/COUTI INST_3/COUTI INST_3/COUTI INST_5/COUTI INST_5/COUTI INST_6/COUTI INST_6/COUTI INST_3/Mxor_SI_Resu. INST_3/Mxor_SI_Resu. INST_5/Mxor_SI_Resu. INST_5/Mxor_SI_Resu. INST_5/Resu. INST_7/COUTI	LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3			P0	Connection	is Move Nets
RC<1> RC<2> RC<3> RC<4> RC<5> RC<6> SUM_1_OBUF SUM_2_OBUF SUM_2_OBUF SUM_3_OBUF SUM_6_OBUF SUM_6_OBUF SUM_6_OBUF SUM_6_OBUF SUM_6_OBUF SUM_6_OBUF	INST_IACOUTI INST_IACOUTI INST_3/COUTI INST_3/COUTI INST_5/COUTI INST_6/COUTI INST_6/COUTI INST_6/COUTI INST_1Mxor_SL Resu. INST_3/Mxor_SL Resu. INST_3/Mxor_SL Resu. INST_6/Mxor_SL Resu. INST_6/Mxor_SL Resu. INST_7/Mxor_SL Resu. INST_7/COUTI INST_7/COUTI INST_7/COUTI	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3	LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3 LUT3			<b>P0</b>	Connection	IS Move Nets

Picture 8: Menu 5.2 Modify Connections: Trigger Data Signals

Return to Project Navigator

Click **OK** to return to menu 5, and from there with to ISE main menu, by saving the settings with the same file name .

Save Pr		×
?	Save Project and return to Project Navigat	or?
	Ja <u>N</u> ein	
Picture	9: saving "Core" project	

Next, the implementation is started and the Spartan 3 board is programmed. During this action, you must watch to make sure that the progress bar runs steadily to the end. Otherwise, close "ChipScope" and "Impact" (without saving) and start "Impact" again.

#### 1.4 <u>Start of "ChipScope"</u>

After installing "ChipScope", ISE shows a new line in the Process window:

Analyze Design Using Chipscope Picture 10: Header of "ChipScope"

Double-click to start,,ChipScope".

The main window of "ChipScope Pro" opens:

🕼 ChipScope Pro Analyzer [new project]	
<u>Eile View J</u> TAG Chain <u>Device Window H</u> elp	
TAO Chain ChipScope PI	 10
	0%
Picture 11: "ChipScope" main window	

First, the JTAG connection must be made: JTAG Chain → Xilinx parallel Cable :

()) Chiefe	
<u>Eile V</u> iew	JTAG Chain Device Window Help
#	Server Host Setting
New Project	JTAG Chain Setup
JTAG Chain	Xilinx Parallel Cable     Xilinx Multil INX Serial Cable
	Xilinx MultiLINX USB Cable
A. W	Oragilent E5904B Cable
	Get Cable Information
Picture 12	$2 \rightarrow ITAG Chain \rightarrow Xiliny Parallel Cable$
In the n	ext menu choose $\rightarrow$ Xilinx Parallel IV and click OK.
ChinScou	ne Pro Analyzer [new project]
Cimpseo	
?	-Parallel Cable Selection
	🔾 Xilinx Parallel III
	Xiiinx Parallel IV
	Auto Detect Cable Type
	-Barallal Cable Parametere-
	Faraller Capie Faralleters
	Speed: Port:
	5 MHz VIPT1 V
	OV Abbroken
Picture 13	3: Parallel Cable Selection
Ignore t	the "Windows Firewall Alert" message that appears and close it with OK:
谢 Wind	ows Security Alert
	To help protect your computer, Windows Firewall has blocked
	some features of this program.
v	
Your co	mputer administrator can unblock this program for you.
	Name: <b>cse</b>
	Publisher: Unknown
	For this program, don't show this message again
3	
Windows	Firewall has blocked this program from accepting connections from the
Internet c	or a network. If you recognize the program or trust the publisher, you can
unblock i	t. <u>When should Lunblock a program?</u>
Picture 1/	1. Windows Firewall Alert" message
$\Delta$ new 1	menu windows income Anne message
	mente window appears, deserioning the detected device.
ChipSc	ope Pro Analyzer 🛛 🔀
	Chain Device Order
Jack	
Inde	x Name Device Name IR Length Device IDCODE USERCODE
	0 myDentee  re30400  0  0141t033
	I duanas di sa
	Auvanced >>
	OK Cancel Read USERCODEs
Picture 1.	5. Device detection

Quit with **OK**; the trigger window, the data window and the console window appear in the main window:

ChipScope Pro Analyzer [new	project]							
<u>F</u> ile <u>V</u> iew <u>J</u> TAG Chain <u>D</u> evice	<u>T</u> rigger Setup W <u>a</u> vefori	m <u>V</u>	⊻indow	<u>H</u> elp				
🟥 🕑 🕨 🖿 T! 🛇 영 위	9 9 9 B							
New Project	😰 Trigger Setup - DI	:V:0 N	MyDevia	:e0 (XC3S400) UNIT:0	MyILAO (ILA)		<b>.</b>	a^ 🖂
JTAG Chain - DEV:0 MyDevice0 (XC3S400)	Match Unit		Functi	on	Value	Ra	Counter	
- Trigger Setup	Add Active		Triaa	er Condition Name		Trigger Condition Equation	n	
	Del O		Tr	ggerCondition0		MO		
Signals: DEV: 0 UNIT: 0 P Data Port	ନ୍ଥି Type: Window	-	Wi	ndows: 1	Depth: 512	Position:	0	
🗠 Trigger Ports	Waveform - DEV:0	) MyD	)evice0	(XC3S400) UNIT:0 Myl	LAO (ILA)		ם נו	a^ 🖂
	Bus/Signal	х	0					
	DataPort[0]	0	0					1
	- DataPort[1]	0	0					
	- DataPort[2]	0	0					
	- DataPort[3]	0	0					
	- DataPort[4]	0	0					
	DataPort[6]	0	0					
	DataPort[7]	0	0					
	- DataPort[8]	0	0					
	- DataPort[9]	0	0					
	- DataPort[10]	0	0					Ļ
		• •	4 🕨 4					•
				X: 0	• 0: 0	▲► Δ(X-0): 0	)	
INFO: Driver vnc4dnrr sys version = 1	040							
INFO: LPT base address = 0378h. INFO: Cable Type = 1, Revision = 3. INFO: Setting cable speed to 5 MHz.								Ē
INFO: Successfully opened Xilinx Par INFO: Cable: Parallel IV, Port: LPT1, S	allel Cable Speed: 5 MHz							=
INFO: Found 1 Core Unit in the JTAG	device Chain.							-

Picture 16: "ChipScope " main window after device detection took place

The last line in the console window is important:

**INFO Found 1 Core Unit found in the JTAG device Chain** If it reads: Found 0 Core Unit found ... then "ChipScope" and "Impact" must be closed and programmed again.

In order to see your own signal names in the Waveform List, you can overwrite these (DataPort(0), etc.) and save them as  $\sim$ .cpj :  $\rightarrow$  File  $\rightarrow$  Save Project.

		ChipScope Pro		re Project As		? 🔰
		Save in:	🔁 b4		· · · ·	•
		2	projnav			
ChipScope Pro A	nalyzer [adder8	Recent				
<u>File View J</u> TAG Ch	iain <u>D</u> evice <u>T</u> ri	g 🔂	L XSC			
New Project	10000	Desktop				
Open Project		<b>G</b>				
<u>S</u> ave Project		My Documents				
S <u>a</u> ve Project As	XC3S400)	Mat 💭				
Page Setup	(ILA) up	My Computer				
<u>P</u> rint		- C				
Import		My Network Places	File name:	adder8.cpj	•	Save
Export	0		Save as type:	Alle Dateien (*.*)	•	Cancel
Picture 17. Save Pro	iect as	Picture 18	Save mer	u: save as ~ cpi		

A complete project file can be loaded with  $\rightarrow$  File  $\rightarrow$  Open Project: As a result you can see the changed signal names:

<u>File View J</u> TAG Chain <u>D</u> evice	<u>T</u> rigger Setup	VV <u>a</u> vefo	orm
New Project	999	R	
Open Project			
<u>S</u> ave Project	Vaveform - DEV	/:0 MyD	evic
S <u>a</u> ve Project As	Bus/Signal	x	0
Pa <u>q</u> e Setup	SOM[0]	0	0
Print	5UM[1]	0	0
Import Evnort	UM[2]	0	0
4 DùloEuradàDD (Santala dalo ani	JUM[3]	0	0
2 D:\ISEwork\BB4\b4\adder8.cpj	5UM[4]	0	0
Exit	UM[5]	0	0
	SUM[6]	0	0
	SUM[7]	0	0
-	SUM[8]	0	0
	A[0]	0	0
	CIN	0	0

In the trigger window, you can indicate a trigger condition. If everything is marked with ,X',

click on **b** to start the data intake.

2	🍘 Trigger Setup - DEV:0 MyDevice0 (XC3S400) UNIT:0 MyILAO (ILA) 🛛 🗖 🖉 🛛										
×		Match Unit	Function	Value Radix Count							
atch	• MO	TriggerPort0	==		>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	Bin	disabled	÷			
Ę	Add Active Trigger C			ondition Name	Trigger Conditi	tion Equation					
ġ	Del	۲	Trigge	erCondition0	MO						
► Cap	Type:	Window	Windows	:1 D	epth: 512 💌 Position	n:	0				

Picture 20: Trigger setup

The X-cursor and an O-cursor in the upper left corner below the trigger-cursor can be fetched , displaced and the number of sample in between can be read :

1	Waveform - DEV:0	) MyC	evic)	:e0 (	XC3S40	10) UNI	T:0 Myll	.AO (IL/	V							័ពីធ	
	Bus/Signal	х	0		40 .0.1	80	120	160	200	<b>240</b>	280	320	360	<b>400</b>	440	480	_
	- sum[0]	0	1														
	(	<b>4 )</b>	4 🕨	4													Þ
					X	75		••	0:	25		• •	Δ(X-	0): 50	)		

Picture 21: X-Cursor and O-Cursor

You can make use of the buttons "Go to X-Cursor", "Go to O-Cursor" and "Zoom in" and "Zoom out":



## **Appendix A:**

#### Usage of the frequency multiplication through the DCM-module

To start the "DCM-Wizard" (building menu) you must first select the menu item IP (CoreGen & Architecture Wizard) with  $\rightarrow$  **Project**  $\rightarrow$  **New Source**; give a file name and activate the "Add to Project" option. Click Next > to continue, and choose "Single DCM v7.1i".

	×	Select Core Type	×
BMM File ChipScope Definition and Connection Embedded Processor Implementation Constraints File File Nam add8 Im MEM File Schematic State Diagram Test Bench Waveform User Document Verilog Module Verilog Test Fixture VHDL Library VHDL Library VHDL Module	ne: n: work\BB1\b1	Basic Elements     Clocking     Clocking     Clock Forwarding / Board Deskew v7.1i     Clock Forwarding / Board Deskew v7.1i     Clock Switching with Two DCMs v7.1i     Clock Switching with Two DCMs v7.1i     Single DCM v7.1i     Digital Signal Processing     Math Functions	
Back Next >	Cancel Help	< Back Next > Cancel	Help
Picture 1_A: New Source		Picture 2_A: Select Core Type	
with Next > a summary comes up.			
New Source Information			
Project Navigator will create a new skeleton	source with the		
following specifications:			
Source Name: add8.xaw			
Source Directory: D:\ISEwork\BB1\b	51		
< Back Finish	n Cancel Help		
Picture 3_A: New Source Inform	nation		
	IVI-VVIZATU ADDEALS		
Check I misit? und the De			
ilinx Clocking Wizard - General Setup		Xilinx Clocking Wizard - Clock Buffers	×
ilinx Clocking Wizard - General Setup		Clock Buffers	×
ilinx Clocking Wizard - General Setup CLKIN CLK0 CLKFB CLK90 CLK180 CLK180		Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Use Global Buffers for all selected clock outputs Clock stomize buffers	×
ilinx Clocking Wizard - General Setup CLKIN CLK0 CLKFB CLK90 CLK70 CLK70		XIIinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Clock Buffers for all selected clock outputs Customize buffers	X
ilinx Clocking Wizard - General Setup CLKIN CLK0 CLKFB CLK90 CLK70 CLK270 CLK02		Xilinx Clocking Wizard - Clock Buffers       Clock Buffer Settings       © Use Global Buffers for all selected clock outputs       © Customize buffers       Input I0       Input I1	×
CLKDR FINISH - CHIC FIC ilinx Clocking Wizard - General Setup CLKIN CLK20 CLK5B CLK20 CLK270 CLK22X CLK22X CLK22X180		XIIinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Customize buffers for all selected clock outputs Customize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer	×
CLKIN CLK20 CLKIN CLK90 CLKFB CLK90 CLK70 CLK270 CLK278 CLK2780 CLK2780 CLK2780 CLK274		Xilinx Clocking Wizard - Clock Buffers       Clock Buffer Settings       Cuse Global Buffers for all selected clock outputs       Customize buffers       Input I0       Input I1       View/Edit Buffer       CLK0       CLKFX	×
CLKIN CLK0 CLKIN CLK0 CLKIN CLK0 CLKFB CLK90 CLK2 CLK2X180 CLK2X180 CLK2X180 CLK7X180		Xilinx Clocking Wizard - Clock Buffers       Clock Buffer Settings       Use Global Buffers for all selected clock outputs       Customize buffers       Input 10       Input 10       CLK0       Global Buffer       CLKPX	×
CLKIN CLKD CLKIN CLKO CLKFB CLK90 CLKFB CLK90 CLK270 CLK270 CLK2X180 CLK2X180 CLK7X180 CLX7X180		Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Customize buffers Input 10 Input 11 View/Edit Buffer CLK0 Global Buffer CLKPX Global Buffer	X
CLKIN CLKO CLKIN CLKO CLKIN CLKO CLKFB CLK90 CLK70 CLK270 CLK270 CLK270 CLK2780 CLK2780 CLK2780 CLK2780 CLK74180		Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Customize buffers for all selected clock outputs Customize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer CLKPX Global Buffer	X
CLKIN CLKO CLKIN CLKO CLKIN CLKO CLKFB CLK90 CLK70 CLK270 CLK270 CLK274 CLK2780 CLK2780 CLK2780 CLK780 CLK780 CLKF780 CLK780 CLK780 CLK780 CLK780 CLK780 CLK780 CLK780 CLK790 CLK270 CLK20 CLX20 CL		Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Customize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer CLKPX Global Buffer	X
CLKIN CLKN CLK9 CLKIN CLK9 CLKFB CLK90 CLK70 CLK70 CLK270 CLK274 CLK274 CLK27480 CLK27480 CLK27480 CLK27480 CLK7480		Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Customize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer CLKFX Global Buffer	X
CLKIN     CLKN     CLK0       CLKIN     CLK0       CLKFB     CLK10       CLK270     CLK270       PSEN     STATUS       STATUS     STATUS       PSEN     STATUS       STATUS     STATUS		Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffers for all selected clock outputs C Customize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer CLKFX Global Buffer	X
CLKIN     CLKN     CLK90       CLKFB     CLK90       CLK70     CLK270       CLK2X     CLK2X       CLK2X     CLK2X       CLK2X     CLK2X       CLK2X     CLK2X       CLK2X     CLK2X       Value:     0       Imput Clock Frequency     Phase Shift       Type:     NDNE       Value:     0       Imput Clock Frequency     0	x 0.000 Degrees	Xilinx Clocking Wizard - Clock Buffers  Clock Buffer Settings  Customize buffers Input I0 Input I1 View/Edit Buffer  CLK0 Global Buffer  CLKFX Global Buffer	X
CLKIN     CLKIN     CLK0       CLKIN     CLK0     CLK0       CLKFB     CLK10     CLK10       CLK2X     CLK2X     CLK2X10       CLK2X180     CLK2X180     CLK7180       V     RST     PSEN     STATUS       PSEN     STATUS     PSDONE       Input Clock Frequency     Phase Shift     Type:       10     ✓ 0     ✓ 0.000 r       CLKIN Source     Feedback Source	Image: state of the s	Xitinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffers for all selected clock outputs C Customize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer CLKFX Global Buffer	X
CLKIN       CLKIN         CLKIN       CLK30         CLKFB       CLK30         CLK70       CLK270         CLK270       CLK270         PSEN       STATUS         PSINCOEC       LOCKED         PSCLK       PSDONE         Source       Phase Shift         Type:       NONE         Value:       0         CLKIN Source       Centernal         CLKIN Source       Centernal         External       C	C None	Xitinx Clocking Wizard - Clock Buffers  Clock Buffer Settings  Customize buffers  Input I0 Input I1 View/Edit Buffer  CLK0 Global Buffer  CLKFX Global Buffer	X
CLKIN       CLKIN         CLKIN       CLK30         CLKFB       CLK30         CLK2X180       CLK2X180         CLK2X180       CLK2X180         CLK70       CLK2X180         CLK70       CLK2X180         CLK2X180       CLK7X180         PSEN       STATUS         PSINCOEC       LOCKED         PSCLK       PSDONE         Source       Phase Shift         Type:       NONE         Value:       0         CLKIN Source       C External         CLKIN Source       C External         Single       Feedback Source	C None	Xilinx Clocking Wizard - Clock Buffers  Clock Buffer Settings  Customize buffers  Input I0 Input I1 View/Edit Buffer  CLK0 Global Buffer  CLKFX Global Buffer	X
Clinx Clocking Wizard - General Setup         CLKIN       CLK0         CLKFB       CLK10         CLK70       CLK10         CLK200       CLK200         CLK100       CLK1000         PSCLX       PSDONE         PSCLX       PSDONE         Value:       0       = 0.000 r.         CLKIN Source       External       Internal         © Single       C Differential       C Internal	C None	Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Clock Buffers for all selected clock outputs Clustomize buffers Input 10 Input 11 View/Edit Buffer CLK0 Global Buffer CLKPX Global Buffer	X
Itinx Clocking Wizard - General Setup         CLKIN       CLK30         CLKFB       CLK30         CLK70       CLK200         CLK200       CLK270         CLK200       CLK200         F85       STATUS         PSEN       STATUS         PSCL       PSDONE         Input Clock Frequency       Phase Shift         Type:       NONE         Value:       0         CLKIN Source       External         CLKIN Source       External         CLKIN Source       External         Clkins Source       External         Clkins Source       External         Cliferential       Feedback Source         Clkins By Value       Feedback Value	C None	Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Clock Buffers for all selected clock outputs Clustomize buffers Input 10 Input 11 View/Edit Buffer CLK0 Global Buffer CLKPX Global Buffer	×
Itinx Clocking Wizard - General Setup         CLKIN       CLK30         CLKFB       CLK30         CLK70       CLK20         CLK2X180       CLK2X180         CLK70       CLK70         CLK2X180       CLK72         FSEN       STATUS         PSEN       STATUS         PSEN       STATUS         PSEN       STATUS         PSCLC       PSDONE         CLKIN Source       External         Clifferential       Differential         Differential       Feedback Value         Clifferential       Feedback Value	C None	Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Clustomize buffers Input 10 Input 11 View/Edit Buffer CLK0 Global Buffer CLKPX Global Buffer	×
Clinix Clocking Wizard - General Setup         CLKIN       CLK30         CLKFB       CLK30         CLK70       CLK20         CLK2X180       CLK2X180         Value       CLK70         PSEN       STATUS         PSEN       STATUS         PSEN       STATUS         PSEN       STATUS         PSEN       STATUS         PSCLC       PSDONE         Value:       0         CLKIN Source       External         Single       0         Differential       Feedback Source         Olide By Value       Feedback Value         Image:       Type:         Value:       0         Image:       Clifferential	C None	Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Clock Buffers for all selected clock outputs Clustomize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer CLKPX Global Buffer	×
Clinix Clocking Wizard - General Setup         CLKIN       CLK30         CLKFB       CLK30         CLK70       CLK20         CLK200       CLK270         CLK200       CLK200         PSEN       STATUS         PSEN       STATUS         PSEN       STATUS         PSINCOEC       LOCKED         PSCL       PSDONE         Value:       0         ©       MH2<		Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Clock Buffers for all selected clock outputs Clustomize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer CLKFX Global Buffer	More Inío
Clinix Clocking Wizard - General Setup         CLKIN       CLK30         CLKFB       CLK30         CLK70       CLK20         CLK200       CLK270         CLK200       CLK200         F85       STATUS         PS1NC0EC       LOCKED         PS0000       PS0000         CLKIN Source       Phase Shift         Type:       NONE         Value:       0         CLKIN Source       External         Single       Differential         Differential       Feedback Source         Oilde By Value       External         Image Duty Cycle Correction       Adva		Xilinx Clocking Wizard - Clock Buffers Clock Buffer Settings Clock Buffer Settings Clock Buffers for all selected clock outputs Clustomize buffers Input I0 Input I1 View/Edit Buffer CLK0 Global Buffer CLKFX Global Buffer	More Info
Itinx Clocking Wizard - General Setup         CLKIN       CLK30         CLKFB       CLK30         CLK270       CLK200         CLK270       CLK270         CLK2X180       CLK2X180         Value       PSEN         STATUS       PSINCDEC         PSINCDEC       LOCKED         PSINCDEC       DIGENDAL         Value       Type:         NONE       External         © Differential       Differential         Differential       Tx< 2x		XIIinx Clocking Wizard - Clock Buffers  Clock Buffer Settings  Clock Buffer Settings  Clustomize buffers  Input I0 Input I1 View/Edit Buffer  CLK0 Global Buffer  CLKFX Global Buffer	More Info

Picture 4\_A: Clocking Wizard 1

Picture 5\_A: Clocking Wizard 2

Xilinx Clocking Wizard - Clock Frequency Synthesizer	Xilinx Clocking Wizard - Summary
Valid Ranges for Speed Grade -5           DFS         Fin (MHz)         Fout (MHz)           Low         1.000 - 326.000         18.000 - 210.000           High         1.000 - 326.000         210.000 - 326.000	Feature Summary: A single DCM configured
Inputs for Jitter Calculations Input Clock Frequency: 50.000 MHz Use output frequency: 320 MHz Cns C Use Multiply (M) and Divide (D) values: M 4 D 1 C	File Directory:         D'NSEwork/AA1\a1         ArchWiz file:       DCM_300.xaw         Block Attributes:         Attributes for DCM, blkname = DCM_INST         CLK_FEEDBACK = 1X         CLKPC_DIVIDE = 5         CLKPX_DIVIDE = 5         CLKPX_VIII TIEV Y = 22
Calculate Generated Output M D Output Period Jitter Period Jitter Frequency (unit interval) (pk-to-pk ns) (MHz) 32 5 320 0.23 0.72	CLINT_MIDEL #32 = FALSE CLKIN_DIMDE_BY_2 = FALSE CLKIN_PHASE_SHIFT = NONE DESKEW_ADJUST = SYSTEM_SYNCHRONOUS DFS_FREDUENCY_MODE = HIGH DLL_FREDUENCY_MODE = LOW DUTY_CYCLE_CORRECTION = TRUE FACTORY_JF = 15hC080 PHASE_SHIFT = 0 STARTUP_WAIT = FALSE
More Info  Kext > Cancel	Show all modifiable attributes     Show only the modifiable attributes whose values differ from the default        < Back
Picture 6_A: Clocking Wizard 3 After this, the read-file ~ xaw is attached to the project:	Picture 7_A: Clocking Wizard 4
Source Pictu	es in Project: a1.ise xc3s400-5tq144 add8-behave (\adder_8.vhd) add8-behave (\adder_8.vhd) \add8_spartan3board2.ucf \add8_spartan3board2.ucf \add8-behaviour (\adder1.vhd) \add8-behaviour (\adder1.vhd) \add8-behaviour (\adder1.vhd) \add8-behaviour (\adder1.vhd) \add8-behaviour (\adder1.vhd) \add8-behaviour (\adder1.vhd) 
Corresponding VHDL source code is also generated in the work marking DCM_300(DCM_300.xaw) and clicking "View HDL-S Sources in Project al.ise al.ise add8-behave (.\adder_8.vhd)	<pre>ing folder; this can be viewed in the "Processes for Source" window by Source". hents.ALL; late_on</pre>
Add8.cot     Add8.spatra.bboard2.ucf     GLKIN_IN     CLKIN_Start_IN     Add1-behaviour(\adde1.vhd)     Add1-behaviour(\ad	<pre>v : in std_logic; : in std_logic; JT : out std_logic; BUFG_OUT : out std_logic; r : out std_logic; DUT : out std_logic;;</pre>

	S/ End DCh_300;
Processes for Source: "DCM_300"	38
Add Existing Source	39 architecture BEHAVIORAL of DCM_300 is
Create New Source	40 signal CLKFB_IN : std_logic;
Create Schematic Symbol	41 signal CLKFX_BUF : std_logic;
View HDL Source	42 signal CLKIN_IBUFG : std_logic;
View HDL Instantiation Template	43 signal CLKO_BUF : std_logic;
	44 signal GND : std_logic;

Picture 9\_A: Viewing DCM\_300.vhd

Now this DCM-component must be instantiated:

```
architecture BEHAVE of ADD8 is
--Function: To_StdLogic
function To_stdlogic ( b: bit) return std_logic is
   variable result: std_logic;
   begin
   if b='0' then
      RESULT := '0';
   else
      RESULT := '1';
   end if;
   return RESULT;
end To stdlogic;
--Komponentendeklaration- - Portliste
component ADD1
   port(X,Y,CIN : in bit;
     SI,COUT : out bit );
end component;
--Komponente DCM
component DCM 300
          CLKIN_IN : in std_logic;
RST_IN : in std_logic;
CLKFX_OUT : out std_logic;
   port ( CLKIN_IN
           CLKIN_IBUFG_OUT : out std_logic;
           CLK0_OUT : out std_logic;
LOCKED_OUT : out std_logic);
end component;
signal RC : bit_vector( 6 downto 0);
signal GND, CLKFX : std_logic;
begin
N_SYSCLK <= not (to_bit(CLKFX));</pre>
GND <= '0';
--Komponenteninstanziierung
DCM 300 INST : DCM 300
    port map(CLKIN_IN => to_stdlogic (SYSCLK),
              RST IN => GND,
              CLKFX OUT => CLKFX,
              CLKIN_IBUFG_OUT => open,
              CLKO_OUT => open,
LOCKED_OUT => open );
```

```
The DCM_300.vhd instantiates the DCM-module on the Spartan-board.
The divisor/multiplication factor sets the quotient from CLKFX_MULTIPLY
and CLKFX_DIVIDE.
The maximum factor is 32/1, and as seen in the Wizard, the maximum frequency is 326 MHz.
With a division factor of 8/1, a board frequency of 50 MHz can be increased to 392 MHz on most boards.
```

```
DCM_INST : DCM
generic map ( CLK FEEDBACK => "1X",
         CLKDV DIVIDE => 2.000000,
         CLKFX_DIVIDE => 1,
         CLKFX_MULTIPLY => 8,
         CLKIN_DIVIDE_BY_2 => FALSE,
         CLKIN PERIOD => 20.000000,
         CLKOUT_PHASE_SHIFT => "NONE",
         DESKEW ADJUST => "SYSTEM SYNCHRONOUS",
         DFS FREQUENCY MODE => "HIGH",
         DLL_FREQUENCY_MODE => "LOW",
         DUTY_CYCLE_CORRECTION => TRUE,
FACTORY_JF => x"COSO",
         PHASE SHIFT => 0,
         STARTUP_WAIT => FALSE)
   port map (CLKFB=>CLKFB IN,
             CLKIN=>CLKIN IBUFG,
             DSSEN=>GND,
             PSCLK=>GND,
             PSEN=>GND,
             PSINCDEC=>GND,
             RST=>RST_IN,
             CLKDV=>open,
             CLKFX=>CLKFX BUF,
             CLKFX180=>open,
             CLKO=>CLKO BUF,
             CLK2X=>open,
             CLK2X180=>open,
             CLK90=>open,
             CLK180=>open,
             CLK270=>open,
             LOCKED=>LOCKED_OUT,
             PSDONE=>open,
             STATUS=>open);
```

end BEHAVIORAL;

After synthesis, the DCM-module is integrated as follows:

