_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chai	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	cyclone-2	James Br	missin	1348	4			77	##	q11.1	0.33	2.0	9.5	vhdl	16	cp_copyt	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	cyclone-4-6	James Br	missin	1345	4			104	##	q13.1	0.33	2.0	12.7	vhdl	16	cp_copyt	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	arria-2	James Br	missin	604	A			167	##	q13.1	0.33	2.0	45.6	vhdl	16	cp_copyt	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	spartan-3e-	James Br	missin	875	4			79	##	14.7	0.33	2.0	14.9	vhdl	16	cp_copyt	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	spartan-6-3	James Br	missin	619	6			86	##	14.7	0.33	2.0	22.8	vhdl	16	cp_copyt	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	kintex-7-3	James Br	missin	622	6			217	##	14.7	0.33	2.0	57.5	vhdl	16	cp_copyt	yes	asm	N		256	2K	Y				2011	2013	microBlaze data sheets	wishbone extras	
r2000	r2000 Soc	alpha	Abdallah Ellbrahimi	RISC	32	32														verilog															empty tar file	
blue	16-bit CPU Blue	stable	Al Williams	accum	16	16	spartan-3-5	James Br	remov	1025	4			63	##	14.7	0.67	1.0	41.1	verilog	16	topbox	web		N		4K	4K	N	16	2		2009	2010		Caxton Foster's Blue derivative	http://www.youtube.com/watch?v=d
vtach	VTACH Bell Labs	mature	Al Williams		13	12	spartan-3-4	James Br	Brakefiel	557	4			71	##	14.7	0.50	1.0	64.1	verilog	16	vtach			N		256	256	Y				2013	2014		ISE project only, BCD arithmetic	
vtach	VTACH Bell Labs	mature	Al Williams		13	12	kintex-7-3	James Br	xilinx core pro		6					14.7	0.50	1.0		verilog	16	vtach			N		256	256	Y				2013	2014		ISE project only, BCD arithmetic	
altium/TSK165x		proprietar	Altium	PIC16	8	12	cyclone-2	Altium		428	4			50			0.33	1.0	38.6	not avail			yes	yes	N	Y	256	4K	Y				2004		CR0140.pdf, CR0114.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
altium/TSK165x		proprietar	Altium	PIC16	8	12	spartan-3-5	Altium		416	4			50			0.33	1.0	39.7	not avail			yes	yes	N	Y	256	4K	Y				2004		CR0140.pdf, CR0114.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
altium/TSK3000A		proprietar	Altium	RISC	32	32	cyclone-2	Altium		2664	4		6	50			1.00	1.0	18.8	not avail			yes	yes	N	N	4G	4G	Y				2004		CR0140.pdf, http://tec	asm, C, C++, schem, VHDL & Verilog	default clock: 50MHz, opt mult/div
altium/TSK3000A		proprietar	Altium	RISC	32	32	spartan-3-5	Altium		2426	4		4	50			1.00	1.0	20.6	not avail			yes	yes	N	N	4G	4G	Y				2004		CR0140.pdf, http://tec	asm, C, C++, schem, VHDL & Verilog	default clock: 50MHz, opt mult/div
altium/TSK51A		proprietar	Altium	8051	8	8x	cyclone-2	Altium		2135	4		1	50			0.33	6.0	1.3	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.PDF, CR0115.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
altium/TSK51A		proprietar	Altium	8051	8	8x	spartan-3-5	Altium		1890	4		1	50			0.33	6.0	1.5	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.PDF, CR0115.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
altium/TSK80x		proprietar	Altium	Z80	8	8x	cyclone-2	Altium		2568	4			50			0.33	3.0	2.1	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.pdf, CR0117.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
altium/TSK80x		proprietar	Altium	Z80	8	8x	spartan-3-5	Altium		2558	4			50			0.33	3.0	2.2	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.pdf, CR0117.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
6809_6309	6809_6309_com	beta	Alejandro Paz Schm	6809	8	8x	spartan-6-3	James Br	Brakefiel	2061	6			109	##	14.7	0.33	3.0	5.8	verilog	5	MC6809_cpu	yes	yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
6809_6309	6809_6309_com	beta	Alejandro Paz Schm	6809	8	8x	kintex-7-3	James Br	Brakefiel	2207	6			212	##	14.7	0.33	3.0	10.6	verilog	5	MC6809_cpu	yes	yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	Aleksander Osn		91256	4	22	106	39		q13.1	1.00	1.0	0.4	verilog	85	soc	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	running on Terasic DE2-115 board
ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	James Br	Brakefiel	36094	4	4	47	46	##	q13.1	1.00	1.0	1.3	verilog	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
ao486	ao486	beta	Aleksander Osman	x86	32	8x	arria-2	James Br	syntax errors		A				##	q13.1	1.00	1.0		system ve	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
ao486	ao486	beta	Aleksander Osman	x86	32	8x	kintex-7-3	James Br	syntax errors		6				##	14.7	1.00	1.0		system ve	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
ao68000	ao68000	beta	Aleksander Osman	68000	16	16x	arria-2	James Br	Brakefiel	3479	A		6	169	##	q13.1	0.67	3.0	10.8	verilog	1	ao68000	som	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses microcode, instruction prefetch buffer	
aoocs	aoOCS - Wishbo	beta	Aleksander Osman	68000	16	16x	cyclone-3	James Br	pin constraint		4					q13.1	0.67	4.0		verilog	22	aoOCS	som	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses ao68000 core, Amiga chip set emulation (blitter, copper), Minimig alter
openfire_cor	OpenFire Proces	alpha	Alex Marschner, Ste	uBlaze	32	32	kintex-7-3	James Br	empty project		6					14.7	0.33	1.0		verilog	12	openfire_	yes	yes	N	N	4G	4G	Y		32		2007	2009	uBlaze data sheets	"FPGA Proven"	
gl85		stable	Alex Miczo	8085	8	8x	kintex-7-3	James Br	gate level des		6					14.7	0.33	4.0		vhdl	1	i8085	yes	yes	N	N	64K	64K	Y				1993		8085 data sheets	also a TTL implementation in VHDL	
microriscii	MicroRISC II	alpha	Alikat	RISC	32	32														verilog	7	?			N		64K	64K	Y		16	5	2002	2009		very little code	
sayeh_proce	SAYEH educatior	stable	Alireza Haghdoost,	RISC	16	8x	kintex-7-3	James Br	Brakefiel	479	6	1		164	##	14.7	0.67	1.0	229.7	verilog	13	Sayeh	yes		N		64K	64K			32		2008	2009	haghdoost.persiangig.c	simple RISC	
encore	Encore	planning	Aloy Ambergen																	no files												2010	2011			
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		2065	4			160			1.13	1.0	87.2	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1355	A			170			1.13	1.0	141.1	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1050	A			160			1.13	1.0	171.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1355	A			280			1.13	1.0	232.5	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		895	A			310			1.13	1.0	389.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1915	4			130			0.64	1.0	43.2	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1045	A			170			0.64	1.0	103.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1570	A			140			0.64	1.0	56.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1045	A			250			0.64	1.0	152.1	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		1300	A			300			0.64	1.0	146.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1080	4			170			0.15	1.0	23.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		730	A			300			0.15	1.0	61.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		840	A			200			0.15	1.0	35.7	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		730	A			320			0.15	1.0	65.8	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		445	A			340			0.15	1.0	114.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
zpuino	SoC:ZPUino	alpha	Alvaro Lopes	forth	32	8	spartan-6	James Br	source code e		6				##	14.7	1.00	1.0		vhdl	8	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2012	http://alvie.com/zpuin	SoC version of modified ZPU	pipelined
crisc_cpu	CRISC CPU	planning	Andre Adrian	68000 like	16	16x														no files					N		4G	4G	Y	20	15		2011			see opencores web page: both 16-bit & 32-bit registers, 11 addressing mode
af65k		alpha	Andre Fachat	6502	16	8x	kintex-7-3	James Br	syntax errors		6				##	14.7	0.67	4.0		vhdl			yes		N	N							2011			extended 6502 with 16, 32 or 64 bit data	
alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James Br	Brakefiel	298	6			237	##	14.7	0.67	1.0	533.3	vhdl	7	top	some		N		64K	64K	Y		16		2009	2009		lightweight CPU	
avrtinyx61co	avrtinyx61core	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James Br	Brakefiel	1243	6			194	##	14.7	0.33	1.0	51.5	vhdl	1	mcu_core		yes	N		64K	128K	Y		32		2008	2009	AVR data sheets		
t51	T51 mcu	stable	Andreas Voggenede	8051	8	8x	kintex-7-3	James Br	Brakefiel	1942	6	1		147	##	14.7	0.33	4.0	6.2	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
t51	T51 mcu	stable	Andreas Voggenede	8051	8	8x	kintex-7-3	James Br	Brakefiel	1921	6	1	2	127	##	14.7	0.33	4.0	5.5	vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	8052 SoC
t51	T51 mcu	stable	Andreas Voggenede	8051	8	8x	arria-2	James Br	proba	3049	6	1		111	##	q13.1	0.33	4.0	3.0	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
t51	T51 mcu	stable	Andreas Voggenede	8051	8	8x	arria-2	James Br	proba	4704	6	1	1	89	##	q13.1	0.33	4.0	1.6	vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	8052 SoC
nige_machine		stable	Andrew Read	forth	32	8	kintex-7-3	James Br	Brakefiel	5033	6	8	33	123	##	14.7	1.00	1.0	24.5	vhdl	29	Board	yes	yes	N		16M	16M		512	512			2014			standalone Forth system	
nige_machine		stable	Andrew Read	forth	32	8	kintex-7-3	James Br	too m	3381	6	8	1		##	14.7	1.00	1.0		vhdl	29	CPU	yes	yes	N		16M	16M		512	512			2014			standalone Forth system	
openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	spartan-3-5	James Br	Brakefiel	1352	4	3	6	39	##	14.7	1.00	1.0	28.8	verilog	27	openfire_	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's OpenF
openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	kintex-7-3	James Br	Brakefiel	1201	6	3	2	105	##	14.7	1.00	1.0	87.4	verilog	27	openfire_	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's OpenF
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera		4500	A			1050			2.50	1.0	583.3	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & c
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	cyclone V	altera		4500	A			925			2.50	1.0	513.9	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & c
ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	zynq	xilinx		4500	6			1000			2.50	1.0	555.6	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	xilinx plan ahead: an A	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & c
t400	*T400 uControlle*	stable	Arnim Laeuger	COP400	4	8x	cyclone-1	Arnim Laeuger		583	4		2	59			0.17	4.0	4.3	vhdl	53	t400_cor	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
t400	*T400 uControlle*	stable	Arnim Laeuger	COP400	4	8x	spartan-2	Arnim Laeuger		643	4		2	60			0.17	4.0	4.0	vhdl	53	t400_cor	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
t48	*T48 uController*	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuger		738	4		1	59			0.33	4.0	6.6	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
t48	*T48 uController*	stable	Arnim Laeuger	MCS-48	8	8x	spartan-2	Arnim Laeuger		771	4		1	30			0.33	4.0	3.2	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
edu_3bus_ar	Educational 3 Bu	spec	Ayman Mohamed	RISC	32	32														no files										33	32		2012	2013			

4stack		simulation	Bernd Paysan	forth	32	5	kintex-7-3	James Br	source errors		6				##	14.7	0.67	1.0		verilog	80	4stack	yes	yes	Y								2002	2011	bernd-paysan.de/b16.html		
b16		stable	Bernd Paysan	forth	16	5	arria-2	James Brakefield			A					q13.1	0.67	1.0		verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16.	two versions: one/15 source files, derived from c18	
b16		stable	Bernd Paysan	forth	16	5	spartan-3-5	James Brakefield			4					14.7	0.67	1.0		verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16.	two versions: one/15 source files, derived from c18	
b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakefiel		554	6			134	##	14.7	0.67	1.0	161.7	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16.	two versions: one/15 source files, derived from c18	
b16		stable	Bernd Paysan	forth	16	5	kintex-7-3	James Brakefiel	source		6				##	14.7	0.67	1.0		verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16.	two versions: one/15 source files, derived from c18	
lpu	LocationPU	planning	Bkorsedal																	no files													2002	2009		very early: minimal doc	
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	cyclone-2	James Brakefiel		3340	4			50	##	q11.1	0.67	2.0	5.0	verilog	24	pdp11	yes	yes	N	N	64K	64K				8	2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	cyclone-4	James Brakefiel		3439	4			64	##	q13.1	0.67	2.0	6.2	verilog	24	pdp11	yes	yes	N	N	64K	64K				8	2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	arria-2	James Brakefiel		2532	A			126	##	q13.1	0.67	2.0	16.7	verilog	24	pdp11	yes	yes	N	N	64K	64K				8	2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	spartan-3-5	James Brakefiel		3842	4			56	##	14.7	0.67	2.0	4.8	verilog	24	pdp11	yes	yes	N	N	64K	64K				8	2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	spartan-6-3	James Brakefiel		2966	6			64	##	14.7	0.67	2.0	7.3	verilog	24	pdp11	yes	yes	N	N	64K	64K				8	2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/
pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	kintex-7-3	James Brakefiel		3089	6			153	##	14.7	0.67	2.0	16.6	verilog	24	pdp11	yes	yes	N	N	64K	64K				8	2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/
pdp8verilog		stable	Brad Parker	PDP8	12	12	spartan-6-3	James Brakefiel		509	6			162	##	14.7	0.50	2.0	79.5	verilog	18	pdp8	yes	yes	N	N	32K	32K				8	2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/R
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakefiel		505	6			366	##	14.7	0.50	2.0	181.3	verilog	18	pdp8	yes	yes	N	N	32K	32K				8	2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/R
pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James Brakefiel		1117	6			251	##	14.7	0.50	2.0	56.1	verilog	18	top	yes	yes	N	N	32K	32K				8	2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/R
wb_z80	Wishbone High P	stable	Brewster Porcella	Z80	8	8x	kintex-7-3	James Brakefiel		2025	6			144	##	14.7	0.33	3.0	7.8	verilog	4	z80_core	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Guy Hutchison TV80	
cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James Br	case c	367	6			355	##	14.7	0.67	1.0	648.1	vhdl	1	cpu16	yes	asm	N		64K	64K		28			2000			part of eForth?	data width can be expanded
ba22		proprieta	CAST Inc	RISC	32	16x	spartan-6	CAST Inc		1800	6		32	72			1.00	1.0	40.0	not avail							4G	4G			32				www.cast-inc.com		
yellowstar	Yellow Star	stable	Charles Brej	MIPS	32	32			missing declarations											verilog	1	processo	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	MIPS R3000 clone, gate level dsgn	brej.org/yellow_star/
gullwing		simulation	Charles LaForest	forth	32	5														no code			yes	asm	N		4K	4K					2007		BS thesis	virtual stack machines vs RISC	MuP21 clone
octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles LaFores		500	A	1		550			0.67	1.0	737.0	verilog	18	Octavo	yes	asm	N					14	16	10		2012	Octavo: an FPGA-Cent	8 core barrel, adjustable data width	~= performance across word sizes, no
cray1		alpha	Christopher Fenton	cray1	64	16	kintex-7-3	James Brakefiel		13463	6	19	10	127	##	14.7	6.00	1.0	56.6	verilog	46	cray_sys_	yes	yes	Y	N	4M	4M	N		512		2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew-cra
cray1		alpha	Christopher Fenton	cray1	64	16	kintex-7-3	James Br	missing black		6				##	v14.1	6.00	1.0		verilog	46	cray_sys_	yes	yes	Y	N	4M	4M	N		512		2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew-cra
cole_c16		beta	Cole Design & Deve	RISC	16	16	spartan-6-3	James Brakefiel		554	6			298	##	14.7	0.67	7.0	51.4	vhdl	1	core	yes	asm	N		64K	64K	N	20	8		2002	2012		(7) clks per inst, complete SOC	for teaching
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	spartan-6-3	James Brakefiel		6901	6		4	40	##	14.7	0.75	1.0	4.3	verilog	25	a23_core	yes	yes	N		4G	4G	Y			3	2010	2013	ARM7 data sheets	no MMU, shared cache	2048 LUTs used as single port RAM
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakefiel		6409	6		2	82	##	14.7	0.75	1.0	9.6	verilog	25	a23_core	yes	yes	N		4G	4G	Y			3	2010	2013	ARM7 data sheets	no MMU, shared cache	2048 LUTs used as single port RAM
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	spartan-6-3	James Brakefiel		12834	6		8	40	##	14.7	1.05	1.0	3.3	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	4096 LUTs used as single port RAM
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakefiel		12450	6		4	98	##	14.7	1.05	1.0	8.2	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	4096 LUTs used as single port RAM
amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakefiel		7926	6		320	92	##	v14.1	1.05	1.0	12.2	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	2454 LUTs used as single port RAM
ax8	AX8 MCU	stable	Daniel Wallner	AVR	8	16	spartan-6-3	James Br	missing ROM		6					14.7	0.33	1.0		vhdl	14	A90S1200			N		64K	128K	Y		32		2002	2009	AVR data sheets	both A90S1200 & A90S2313	80K LUTs as ROM
ppx16	PPX16 mcu	stable	Daniel Wallner	PIC16	8	14	spartan-6-3	James Br	missing ROM BB							14.7		1.0		vhdl	10	P16C55,	yes	yes	N	Y	256	4K	Y				2002	2009	PIC16 data sheets	both 16C55 & 16F84	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	cyclone-2	James Brakefiel		829	4			84	##	q11.1	0.33	4.0	8.4	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	cyclone-4	James Brakefiel		831	4			110	##	q13.1	0.33	4.0	10.9	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	arria-2	James Brakefiel		617	A			190	##	q13.1	0.33	4.0	25.4	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-3-5	James Brakefiel		923	4			83	##	14.7	0.33	4.0	7.5	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-6-3	James Brakefiel		725	6			128	##	14.7	0.33	4.0	14.5	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakefiel		575	6			291	##	14.7	0.33	4.0	41.7	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
t80	T80 cpu	stable	Daniel Wallner	8080	8	8x	spartan-6-3	James Br	8080 r	958	6			95	##	14.7	0.33	9.0	3.6	vhdl	5	T8080se	yes	yes	N	N	64K	64K	Y				2002	2011	8080 data sheets	Z80, 8080 & gameboy inst sets, several usages	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	arria-2	James Br	xilinx primitive		A				##	q13.1	0.33	3.0		vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-3-5	James Br	Z80 m	1991	4			54	##	14.7	0.33	3.0	3.0	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-6-3	James Br	Z80 m	1462	6			83	##	14.7	0.33	3.0	6.2	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James Br	Z80 m	1389	6			163	##	14.7	0.33	3.0	12.9	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
agcnorm	Apollo Guidance	beta	Dave Roberts	?	16	16												1.0		vhdl	5	AGC	some		N		32M	32M					2010	2012		Apollo Guidance Computer via NOR gate emulation	
Lutiac		custom	David Galloway, Da	reg	16	NA	stratix-4	David Galloway		140	A	4		198			0.67	1.0	947.6	vhdl & verilog								64	N	64	32	3		2010	Lutiac – Small Soft Pro	synthesis maps PC into ucode	no inst mem: small state machine, ~20
Lutiac		custom	David Galloway, Da	reg	16	NA	stratix-4	David Galloway		480	A	4		197			0.67	1.0	275.0	vhdl & verilog						Y		128	N	64	32	3		2010	Lutiac – Small Soft Pro	synthesis maps PC into ucode	no inst mem: large state machine, ~20
free6502		stable	David Kessner	6502	8	8x	spartan-6-3	James Brakefiel		663	6			89	##	14.7	0.33	4.0	11.1	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
free6502		stable	David Kessner	6502	8	8x	kintex-7-3	James Brakefiel		646	6			193	##	14.7	0.33	4.0	24.6	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
elm	ELM Embedded	alpha	David Sheffield, Curt Harting																	no files													2010	2010			
1664	1664 microproce	sim?	Denis Godinho																	C										26			2010	2010		C based simulation only	
theia_gpu	Theia: ray graphi	beta	Diego Valverde	GPU														1.0		verilog	32	Theia	yes	asm	N						12		2011	2012		multi-core, 3D rendering & shader	
mcu8	8-bit microcontr	sim?	Dimo Pepelyashev		8															vhdl	16	processor_E		asm												asm, simulated	
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	cyclone-2	Dinesh Annayya		5072	4			39			0.33	4.0	0.6	verilog	74	oc8051_t	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James Brakefiel		1985	6	1		127	##	14.7	0.33	4.0	5.3	verilog	74	oc8051_t	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
p16		alpha	Don Golding	forth	16	5	kintex-7-3	James Br	bad syntax		6					14.7	0.67	1.0		vhdl	1	p16			N		64K	64K					2000				
pavr	pAVR	alpha	Doru Cuturela	AVR	8	16														vhdl	8		yes	yes	N		64K	64K	Y		32	6	2003	2009	AVR data sheets	simulation only, is ASIC project	
mips_16	Educational 16-b	stable	Doyya Doyya	RISC	16	16	kintex-7-3	James Br	collapsed in co		6					14.7	1.00	1.0		verilog	12	mips_16_	yes		N		64K	64K		13	8	5	2012	2012			
c0or1k	Codezero OpenR	planning	Drasko Draskovic	RISC																no code													2010			C code for simulation	
ensilica		proprietar	ensilica.com	eSi-1600	16		virtex-5	ensilica		1100	6			160			0.67	1.0	97.5	not avail			yes	yes	N		64K	64K			16				www.ensilica.com	verilog source included with license	10 addressing modes
ensilica		proprietar	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200			1.00	1.0	111.1	not avail			yes	yes			4G	4G			16	5			www.ensilica.com	verilog source included with license	10 addressing modes
eric5		proprietar	entner-electronics.c	forth	9	9	cyclone-4-6	enter-electronics.com			4	opt		60			0.67	1.0		not avail							512	128K			3-4		2007			40 MIPS: ERIC5+, ERIC5Q+	
eric5		proprietar	entner-electronics.c	forth	9	8	cyclone-4-6	enter-electroni		110	4	opt		60			0.42	1.0	229.1	not avail							512	1K			3-4		2007			25 MIPS: ERIC5xs, ERIC5Q	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-3	Eric Wallin		1800	4	4	3	200		q13.0	1.00	1.0	111.1	verilog			yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-2	James Brakefiel		1633	4	4	44	169	##	q11.1	1.00	1.0	103.4	verilog		core	yes		N				N	40	10	8	2013	2014		4 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-4	James Brakefiel		3046	4		14	115	##	q13.1	1.00	1.0	37.6	verilog		core	yes		N				N	40	10	8	2013	2014		4 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	James Brakefiel		1256	A	6	3	217	##	q13.1	1.00	1.0	172.5	verilog		core	yes		N				N	40	10	8	2013	2014		4 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	arria-2	James Brakefiel		905	A	8	20	284	##	q13.1	1.00	1.0	313.4	verilog		core	yes		N				N	40	10	8	2013	2014		4 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-2	James Brakefiel		2375	4	4	52	165	##	q11.1	1.00	1.0	69.6	verilog		hive_core	yes		N				N	40	10	8	2013	2014		8 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-4	James Brakefiel		3792	4		29	115	##	q13.1	1.00	1.0	30.5	verilog		hive_core	yes		N				N	40	10	8	2013	2014		8 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	James Brakefiel		1290	A	6	24	177	##	q13.1	1.00	1.0	137.1	verilog		hive_core	yes		N				N	40	10	8	2013	2014		8 symetrical stacks, eight threads via pipeline barrel	
hive	hive	stable	Eric Wallin	4-8 stack	32	16	arria-2	James Brakefiel		1387	A	8	24	283	##	q13.1	1.00	1.0	204.4	verilog		hive_core	yes		N				N	40	10	8	2013	2014		8 symetrical stacks, eight threads via pipeline barrel	

hive	hive	stable	Eric Wallin	4-8 stack	32	16	spartan-6-3	James Br	missing port n	6				##	14.7	1.00	1.0		verilog		core	yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	spartan-3e-	James Brakefiel	385	4		2	59	##	14.7	0.11	3.0	5.7	verilog	12	natalius_	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakefiel	232	6		1	175	##	14.7	0.11	3.0	27.7	verilog	12	natalius_	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
s1_core	S1 Core	stable	Fabrizio Fazzino eta	SPARC	64	32	arria-2	James Br	syntax errors	A				##	q13.1	2.00	1.0		verilog	136	s1_top	yes	yes	Y	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	
s1_core	S1 Core	stable	Fabrizio Fazzino eta	SPARC	64	32	kintex-7-3	James Brakefiel	54434	6	8	57	50	##	14.7	2.00	1.0	1.8	verilog	136	s1_top	yes	yes	Y	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	ISE run
s1_core	S1 Core	stable	Fabrizio Fazzino eta	SPARC	64	32	kintex-7-3	James Brakefiel	52845	6	8	59	56	##	v14.1	2.00	1.0	2.1	verilog	136	s1_top	yes	yes	Y	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	Vivado run
m1_core	M1 Core	beta	Fabrizo Fazzino, Alb	MIPS?	32	32	cyclone-2	James Brakefiel	3752	4			70	##	q11.1s	1.00	1.0	18.8	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Alb	MIPS?	32	32	cyclone-4	James Brakefiel	3795	4			94	##	q13.1	1.00	1.0	24.8	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Alb	MIPS?	32	32	arria-2	James Brakefiel	2101	A			190	##	q13.1	1.00	1.0	90.6	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Alb	MIPS?	32	32	spartan-3-5	James Brakefiel	4688	4			70	##	14.7	1.00	1.0	14.9	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Alb	MIPS?	32	32	spartan-6-3	James Brakefiel	3483	6			131	##	14.7	1.00	1.0	37.5	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
m1_core	M1 Core	beta	Fabrizo Fazzino, Alb	MIPS?	32	32	kintex-7-3	James Brakefiel	3456	6			233	##	14.7	1.00	1.0	67.3	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
diogenes	diogenes	beta	Fekknhifer	RISC	16	16	kintex-7-3	James Brakefiel	807	6		1	297	##	14.7	0.67	1.0	246.3	vhdl	11	cpu	yes	yes	N			1K					2008	2009		"student RISC system"	
mc6809e		beta	Flint Weller	6809	8	8x	kintex-7-3	James Br	gate level prin	6					14.7	0.33	3.0		vhdl	26	core_680	yes	yes	N	N	64K	64K	Y				1999		6809 data sheets	course work, ASIC orientation	
t6507lp	T6507LP	beta	Gabriel Oshiro, Sam	6502	8	8x	spartan-6-3	James Br	errors						14.7		4.0		verilog	22	t6507lp	yes	yes	N	N	64K	64K	Y				2009	2010	6502 data sheets	for use in ATARI 2600	
or1200_soc	or1200_soc	beta	gaz	OpenRISC	32	32	cyclone-2	James Br	missing files	4				##	q11.1s	0.67	2.0		verilog	39	top	yes	yes	Y		4G	4G	Y		32			2011		OpenRISC on Terasic DE1 board	
or1200_soc	or1200_soc	beta	gaz	OpenRISC	32	32	arria-2	James Br	undefined ent	A				##	q13.1	0.67	2.0		verilog	39	top	yes	yes	Y		4G	4G	Y		32			2011		OpenRISC on Terasic DE1 board	
or1200_soc	or1200_soc	beta	gaz	OpenRISC	32	32	kintex-7-3	James Br	unknown moc	6				##	14.7	1.00	1.0		verilog	39	top	yes	yes	Y		4G	4G	Y		32			2011		OpenRISC on Terasic DE1 board	
ignite_ptsc		proprietar	George Shaw	forth	32	8											1.0		not avail					N		4G	4G					1995	2002		ShBoom clone, fast ASIC with high coding density	
myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SP-spartan-	James Brakefiel	4494	4		12	67	##	14.7	1.00	1.0	15.0	vhdl	3	theCore	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis, four variants	
myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SP-kintex7-	James Brakefiel	2959	6		6	223	##	14.7	1.00	1.0	75.3	vhdl	3	theCore	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis, four variants	
myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SP-spartan-	Gerhard Hohne	6526	4		14	60	##	i9.2	1.00	1.0	9.2	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesi	8.32 Whetstones
myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SPC-spartar	Gerhard Hohne	8134	4		17	61	##	i9.2	1.00	1.0	7.4	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesi	7.32 Whetstones
myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SPM-sparta	Gerhard Hohne	7275	4	16	14	68	##	i9.2	1.00	1.0	9.3	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesi	25.15 Whetstones
myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SPMC-spart	Gerhard Hohne	9499	4	16	17	53	##	i9.2	1.00	1.0	5.6	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis, four variants	
myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SPMD-spart	Gerhard Hohne	9265	4	16	14	63	##	i9.2	1.00	1.0	6.8	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesi	22.5 Whetstones
cpugen	Cpu Generator	stable	Giovanni Ferrante																													2003	2009		x86 executable that generates VHDL uP	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	cyclone-2	James Brakefiel	6843	4	8		45	##	q11.1s	1.00	1.0	6.6	verilog	20	processo	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	cyclone-4	James Brakefiel	9556	4			48	##	q13.1	1.00	1.0	5.0	verilog	20	processo	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	did not infer multipliers
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	arria-2	James Brakefiel	3716	A	8		79	##	q13.1	1.00	1.0	21.3	verilog	20	processo	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	spartan-3-5	James Brakefiel	6322	4	8		38	##	14.7	1.00	1.0	6.0	verilog	20	processo	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	spartan-6-3	James Brakefiel	4823	6	8		43	##	14.7	1.00	1.0	8.8	verilog	20	processo	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	kintex-7-3	James Brakefiel	4822	6	8		90	##	14.7	1.00	1.0	18.6	verilog	20	processo	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
hc11core		stable	Green Mountain Co	68HC11	8	8x	arria-2	James Brakefiel	1962	A			116	##	q13.1	0.33	4.0	4.9	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with correctio	http://www.gmvhdl.com/hc11core.ht
hc11core		stable	Green Mountain Co	68HC11	8	8x	kintex-7-3	James Brakefiel	2190	6			127	##	14.7	0.33	4.0	4.8	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with correctio	http://www.gmvhdl.com/hc11core.ht
tv80	TV80	mature	Guy Hutchison, Hov	Z80	8	8x	cyclone-2	James Brakefiel	2148	4			63	##	q11.1s	0.33	3.0	3.2	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Hov	Z80	8	8x	cyclone-4	James Brakefiel	2193	4			86	##	q13.1	0.33	3.0	4.3	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Hov	Z80	8	8x	arria-2	James Brakefiel	1413	A			139	##	q13.1	0.33	3.0	10.9	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Hov	Z80	8	8x	spartan-3-5	James Brakefiel	2095	4			54	##	14.7	0.33	3.0	2.9	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Hov	Z80	8	8x	spartan-6-3	James Brakefiel	1180	6			83	##	14.7	0.33	3.0	7.8	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
tv80	TV80	mature	Guy Hutchison, Hov	Z80	8	8x	kintex-7-3	James Brakefiel	1207	6			182	##	14.7	0.33	3.0	16.6	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
hivek		alpha	Hadley Magno	VLIW	32												1.0		vhdl	18	hivek											2013			two inst per clock	incomplete source code
hicovec	HiCoVec a config	beta	Harald Manske, Gu	RISC	32	32	kintex-7-3	James Br	compiler erro	6					14.7	1.00	1.0		vhdl	28	cpu	yes	asm	N				Y				2008	2010		hybrid scalar & vector processor	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	cyclone-4-6	James Brakefiel	5153	4			79	##	q13.1	1.00	1.5	10.2	verilog	23	eco32	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakefiel	4564	4		10	51	##	14.7	1.00	1.5	7.4	verilog	23	eco32	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	downloaded ISE project run, has *.ucf
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	cyclone-2	James Brakefiel	4840	4		2	56	##	q11.1s	1.00	1.5	7.8	verilog	17	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	cyclone-4-6	James Brakefiel	5153	4			79	##	q13.1	1.00	1.5	10.2	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	arria-2	James Brakefiel	2711	A			116	##	q13.1	1.00	1.5	28.6	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakefiel	3034	4		2	55	##	14.7	1.00	1.5	12.0	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-6-3	James Brakefiel	2271	6		1	92	##	14.7	1.00	1.5	27.0	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	atrix-7-3	James Brakefiel	2107	6		1	121	##	14.7	1.00	1.5	38.4	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakefiel	2210	6		1	160	##	14.7	1.00	1.5	48.1	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
mc8051		stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James Brakefiel	3022	6	1		83	##	14.7	0.33	4.0	2.3	vhdl	49	mc8051c	yes	yes	N	N	256	64K	Y				1999	2013	www.oreganosystems	fast 8051, version available with floating-point by David Lundgren	
xproz		stable	Herbert Kleebauer	CISC	16	16x											1.0		schematic			yes	asm	N		64K	64K					1995			documentation in German	
edge	Edge Processor (	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	Hesham	unkown modu	6	7		50		14.7	1.00	1.0		verilog	30	edge_atl	yes	yes	N	N	4G	4G	Y		32	5	2014		MIPS data sheets	MIPS1 clone, on Atlys Spartan-6 LX45	
edge	Edge Processor (	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	James Brakefiel	5345	6	7	1	8	##	14.7	1.00	1.0	1.5	verilog	30	edge_cor	yes	yes	N	N	4G	4G	Y		32	5	2014		MIPS data sheets	MIPS1 clone	
df6805		proprietar	Hitech Global	6805	8	8x	stratix-1	Hitech Global	1690	4			83			0.33	4.0	4.1	not avail			yes	yes	N	N	64K	64K	Y						6805 data sheets		www.hitechglobal.com/IPCores/DF68
cpu86		beta	ht-lab.com	8086	8	8x	kintex-7-3	James Brakefiel	3421	6	1		127	##	14.7	0.17	2.0	3.1	vhdl	23	cpu86_tc	yes	yes	N	N	1M	1M	Y				2002	2010	x86 data sheets	8088 clone	www.ht-lab.com
recore54		beta	ht-lab.com	PIC16	8	14	kintex-7-3	James Br	Cannot find <r	6					14.7	0.33	1.0		vhdl	20	rcore54_	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets	PIC16 clone	www.ht-lab.com
iDEA		alpha	Hui Yan Cheah etal	RISC	16	32	virtex-6	Liu Cheah	321	6	1	2	405		13.2	0.67	1.0	845.3	verilog	22	cpu_top	yes	yes	N	Y	64K	64K	N	24	32	9	2011	2014	The iDEA DSP Block Ba	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual r
iDEA		alpha	Hui Yan Cheah etal	RISC	16	32	artic-7	Liu Cheah	324	6	1	2	281		13.2	0.67	1.0	581.1	verilog	22	cpu_top	yes	yes	N	Y	64K	64K	N	24	32	9	2011	2014	The iDEA DSP Block Ba	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual r
iDEA		alpha	Hui Yan Cheah etal	RISC	16	32	kintex-7	Liu Cheah	343	6	1	2	410		13.2	0.67	1.0	800.9	verilog	22	cpu_top	yes	yes	N	Y	64K	64K	N	24	32	9	2011	2014	The iDEA DSP Block Ba	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual r
iDEA		alpha	Hui Yan Cheah etal	RISC	16	32	virtex-7	Liu Cheah	324	6	1	2	378		13.2	0.67	1.0	781.7	verilog	22	cpu_top	yes	yes	N	Y	64K	64K	N	24	32	9	2011	2014	The iDEA DSP Block Ba	uses DSP slice in barrel mode for ALU	GitHub version is simulation only
6502vhdl	6502vhdl	planning	Huyvo	6502	8	8x													C				yes	N	N	64K	64K	Y				2003	2009	6502 data sheets	to have a C program generate VHDL	
6502_verilog	6502_verilog_de	sim?	Hyungok Tak	6502	8	8x													verilog				yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	no files, simulated	
lattice6502	Lattice 6502	beta	Ian Chapman	6502	8	8x	kintex-7-3	James Brakefiel	4942	6			214	##	14.7	0.33	4.0	3.6	vhdl	3	ghdl_pro	yes	yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	targeted to LCMXO2280	huge LUT count
pdp8l	Minimal PDP8/L	beta	Ian Schofield	PDP8	12	12	cyclone-3	James Brakefiel	1088	4		48	63	##	q13.1	0.50	2.0	14.4	vhdl	11	top	yes	yes	N	N	4K	4K					2013		PDP8 data sheets		
v1_coldfire		stable	IPextreme	68000	16	16x	cyclone-3	freescale	5000	4			80			0.89	1.0	14.2				yes	yes	N	N	4G	4G	Y		16		2008		68000 data sheets	free for Cyclone III	http://www.ip-extreme.com/IP/coldfi
J1		stable	James Bowman	forth	16	16	spartan-6	James Brakefiel	333	6		1	117	##	14.7	0.80	1.0	280.2	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx,	uCode inst, dual port block RAM	32 deep data & return stacks
J1		stable	James Bowman	forth	16	16	kintex-7-3	James Brakefiel	387	6		4	133	##	14.7	0.80	1.0	274.6	verilog	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx,	uCode inst, dual port block RAM	32 deep data & return stacks

J1		stable	James Bowman	forth	16	16	kintex-7-3	James Br	syntax errors		6					14.7	0.80	1.0		vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx,	uCode inst, dual port block RAM	32 deep data & return stacks
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	cyclone-2	James Br	2 stag	237	4		1	138	##	q11.1	0.04	1.0	23.3	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	Block ROM inferred in 2 stage pipe ver
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	cyclone-4	James Br	2 stag	238	4		1	138	##	q13.1	0.04	1.0	23.1	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	Block ROM inferred in 2 stage pipe ver
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	arria-2	James Br	2 stag	167	A		1	299	##	q13.1	0.04	1.0	71.7	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	Block ROM inferred in 2 stage pipe ver
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	spartan-3-5	James Br	1 stag	85	4		1	157	##	14.5	0.04	1.0	73.7	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	spartan-6-3	James Br	1 stag	65	6		1	223	##	14.5	0.04	1.0	137.3	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	
lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James Br	1 stag	63	6		1	358	##	14.5	0.04	1.0	227.2	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	
xr16		stable	Jan Gray	RISC	16	16	spartan-2-5	Jan Gray		257	4		2	37			0.67	1.0	96.6	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R
xr16		stable	Jan Gray	RISC	16	16	spartan-2-5	Jan Gray		200	4		2	50			0.67	1.0	167.5	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	handcrafted FPGA layout
xr16		stable	Jan Gray	RISC	16	16	spartan-3-5	James Brakefiel		392	4			80	##	14.7	0.67	1.0	136.2	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
xr16		stable	Jan Gray	RISC	16	16	virtex-4	James Brakefiel		392	4			149	##	14.7	0.67	1.0	254.9	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
xr16		stable	Jan Gray	RISC	16	16	spartan-6-3	James Brakefiel		283	6			98	##	14.7	0.67	1.0	233.2	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, speed mode better
xr16		stable	Jan Gray	RISC	16	16	virtex-5-2	James Brakefiel		288	6			131	##	14.7	0.67	1.0	305.9	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakefiel		273	6			263	##	14.7	0.67	1.0	644.8	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, speed mode better
xr16		stable	Jan Gray	RISC	16	16	spartan-3-5	James Brakefiel		502	4			82	##	14.7	0.67	1.0	109.6	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
xr16		stable	Jan Gray	RISC	16	16	virtex-4	James Brakefiel		511	4			154	##	14.7	0.67	1.0	201.5	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
xr16		stable	Jan Gray	RISC	16	16	spartan-6-3	James Brakefiel		336	6			92	##	14.7	0.67	1.0	183.6	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
xr16		stable	Jan Gray	RISC	16	16	virtex-5-2	James Brakefiel		369	6			136	##	14.7	0.67	1.0	247.8	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakefiel		337	6			202	##	14.7	0.67	1.0	402.0	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode vastly bette
cpu6502_tru	cpu6502_tc	stable	Jens Gutschmidt	6502	8	8x	kintex-7-3	James Brakefiel		1678	6			159	##	14.7	0.33	4.0	7.8	vhdl	7	r6502_tc		yes	N	N	64K	64K	Y				2008	2010	6502 data sheets		
cpu65c02_tru	cpu65c02_tc	stable	Jens Gutschmidt	6502	8	8x	spartan-6-3	James Br	latch v	4794	6			47	##	14.7	0.33	4.0	0.8	vhdl	8	core		yes	N	N	64K	64K	Y				2008	2013	6502 data sheets		
popcorn		stable	Jeung Joon Lee	accum	8	8x	spartan-6-3	James Brakefiel		268	6			171	##	14.7	0.33	1.0	210.9	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
popcorn		stable	Jeung Joon Lee	accum	8	8x	kintex-7-3	James Brakefiel		267	6			347	##	14.7	0.33	1.0	428.4	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
myblaze	myBlaze	mature	Jian Luo	uBlaze	32	32												1.0		myhdl			yes	yes	N		4G	4G	Y		32		2010	2010	microBlaze data sheet	clone, python code generators	
leon		stable	Jiri Gaisler, Jan And	SPARC	32	32				3500								1.0		vhdl	100s	leon3x	yes	yes	Y		4G	4G			64		2003	2013	SPARC data sheets	customized for ~50 FPGA boards, configurable	
rise	RISE Microproce	beta	Jlechner etal	RISC	16	16	kintex-7-3	James Br	missing black		6	1				14.7	0.67	1.0		vhdl	26	rise	yes	asm	N		64K	64K			16	5	2006	2010	en.wikiversity.org/wik	ARM style register usage	
scarts	Scarts Processor	beta	Jlechner, Martin Wa	RISC	16	16	kintex-7-3	James Br	missing signal		6					14.7	0.67	1.0		vhdl	18	scarts		yes	N		64K	64K		122	16	4	2011	2012		GCC compiler	
arm4u	ARM4U	stable	Joanathan Masur, X	ARM7	32	32	cyclone-2	James Brakefiel		2084	4	3	12	43	##	q11.1	0.75	1.0	15.4	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory
arm4u	ARM4U	stable	Joanathan Masur, X	ARM7	32	32	cyclone-4-6	James Brakefiel		2809	4		8	43	##	q13.1	0.75	1.0	11.5	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory
arm4u	ARM4U	stable	Joanathan Masur, X	ARM7	32	32	aria-2	James Brakefiel		1668	A	4	8	66	##	q13.1	0.75	1.0	29.5	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory
ourisc	16-bit Open uRIS	alpha	Joao Carlos		16	16	stratix-4	Joao Carlos		500	A	1		550			0.67	1.0	737.0	vhdl										26			2013	2013		very incomplete source code	
pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Ro	PDP8	12	12	spartan-6-3	James Brakefiel		1332	6	1		81	##	14.7	0.50	2.0	15.1	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Ro	PDP8	12	12	kintex-7-3	James Brakefiel		1219	6	1		183	##	14.7	0.50	2.0	37.5	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
jam		stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakefiel		1369	6			143	##	14.7	1.00	1.0	104.2	vhdl	17	cpu	yes		N	Y	128K	128K			32	5	2002			serial multiply & divide	
risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakefiel		331	6			333	##	14.7	0.33	1.0	332.3	verilog	1	risc16f84	yes	yes	N	Y	256	4K	Y				2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
micro16b		beta	John Kent	accum	16	16	kintex-7	James Brakefiel		205	6			434	##	14.7	0.33	2.0	349.0	vhdl	1	u16bcpu	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome.	very limited inst set	MIPS/clk adj'd, 2 clks/inst
micro16b		beta	John Kent	accum	16	16	spartan-3E-	James Brakefiel		467	4		3	76	##	14.7	0.33	2.0	26.9	vhdl	13	Micro16b	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome.	SOC version, very limited inst set	MIPS/clk adj'd, 2 clks/inst
micro8a		beta	John Kent	accum	8	16	kintex-7	James Brakefiel		531	6			204	##	14.7	0.33	3.0	42.3	vhdl	11	Micro8	yes		N	N	2K	2K	Y				2002	2002	members.optushome.	derived from Tim Boscke's mcpu, not perfected	
system05	SOC:system05	beta	John Kent	6805	8	8x	kintex-7-3	James Brakefiel		834	6			204	##	14.7	0.33	4.0	20.2	vhdl	10	System05	yes	yes	N	N	64K	64K	Y				2003	2009	6805 data sheets		
system09	SOC:system09	stable	John Kent	6809	8	8x	spartan-6-3	James Brakefiel		2127	6			64	##	14.7	0.33	3.0	3.3	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
system09	SOC:system09	stable	John Kent	6809	8	8x	kintex-7-3	James Brakefiel		1945	6			154	##	14.7	0.33	3.0	8.7	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
system11		alpha	John Kent, David Bu	68HC11	8	8x	kintex-7-3	James Brakefiel		1218	6			153	##	14.7	0.33	4.0	10.3	vhdl	17	cpu11	yes	yes	N	N	64K	64K	Y				2003	2009	6811 data sheets	known bugs & untested instructions	
system68	System68	stable	John Kent, David Bu	6801	8	8x	spartan-3-5	James Brakefiel		2235	4		4	46	##	14.7	0.33	4.0	1.7	vhdl	21	cpu68	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets		
jpu16		stable	Joksan Alvarado	RISC	16	26	kintex-7-3	James Br	missing RAM f		6					14.7	0.67	1.0		vhdl	9	JPU16	yes	asm	N		64K	64K			16		2012		https://github.com/jo	32 deep call stack, 8 addressing modes	
leros32	Leros-32	simulation	Jon Pry	accum	32	16	kintex-7-3	James Br	missing memory components											vhdl	10	leros_nexys2			N		4G	4G					2013		https://github.com/jo	see Leros entry, simulation only	missing several dual port RAMs
tinycpu	TinyCPU	alpha	Jordan Earls	RISC	8	16	kintex-7-3	James Br	bit len	1182	6			200	##	14.7	0.33	2.0	28.0	vhdl	10	top		asm	N	N	64K	64K			16		2012	2012			
sub86	Small x86 subset	alpha	Jose Rissetto	8086	8x	8x														verilog	1	sub86	yes	yes	N	N	64K	64K	Y		7		2012	2013		no segment registers, limited op-codes	
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	cyclone-2	Jose Ruiz		2349	4			50		q11.1	1.00	1.0	21.3	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki/	MIPS R3000 clone	originally MIPS-I moving to MIPS32r1
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	spartan-3	Jose Ruiz		3173	4			51		14.3	1.00	1.0	16.1	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki/	MIPS R3000 clone	originally MIPS-I moving to MIPS32r1
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	virtex-5	Jose Ruiz		2017	6			104		14.3	1.00	1.0	51.6	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki/	MIPS R3000 clone	originally MIPS-I moving to MIPS32r1
ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakefiel		1533	6			163	##	14.7	1.00	1.0	106.0	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki/	MIPS R3000 clone	originally MIPS-I moving to MIPS32r1
light52	Lightweight 8051	beta	Jose Ruiz	8051	8	8x	cyclone-2-7	Jose Ruiz		1339	4	1	29	62			0.33	6.0	2.5	vhdl	8	light52_c	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	0.0187 DMIPS/MHz, i8051 is 0.0094 DI
light52	Lightweight 8051	beta	Jose Ruiz	8051	8	8x	spartan-3-4	Jose Ruiz		1424	4	1	10	35			0.33	6.0	1.4	vhdl	8	light52_c	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	~ 6 clocks/inst
light52	Lightweight 8051	beta	Jose Ruiz	8051	8	8x	kintex-7-3	James Brakefiel		1027	6	1	1	148	##	14.7	0.33	6.0	7.9	vhdl	8	light52_c	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to balanced	~ 6 clocks/inst
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Lito	8080	8	8x	spartan-2-5	Jose Ruiz		203	4		4	60		q9.1	0.33	9.0	10.8	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to speed, bare core	typically 9 clocks per inst, .04=.33/9
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Lito	8080	8	8x	cyclone-2-7	Jose Ruiz		413	4		4	80		q9.0	0.33	9.0	7.1	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to balanced, bare core	typically 9 clocks per inst, .04=.33/9
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Lito	8080	8	8x	spartan-3-5	Jose Ruiz		209	4		1	100		q9.1	0.33	9.0	17.5	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to speed, bare core	typically 9 clocks per inst, .04=.33/9
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Lito	8080	8	8x	kintex-7-3	James Brakefiel		154	6		1	247		14.7	0.33	9.0	58.9	verilog	5	i80soc	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, includes UART, inte	typically 9 clocks per inst, .04=.33/9
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Lito	8080	8	8x	spartan-6	James Brakefiel		148	6		3	172	##	14.7	0.33	9.0	42.7	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/9
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Lito	8080	8	8x	kintex-7-3	James Brakefiel		154	6		1	247	##	14.7	0.33	9.0	58.9	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/9
light8080	Lightweight 8080	stable	Jose Ruiz, Moti Lito	8080	8	8x	spartan-6	James Brakefiel		150	6		3	142	##	14.7	0.33	9.0	34.6	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/9
oops	OoOPs Out-of-O	planning	Joshua Smith	MIPS	32	32														verilog	13		yes	yes	N		4G	4G	Y		32		2012	2012		incomplete source code	
c16	16 Bit Microcont	stable	Jsauermann	C	16	8x	spartan-3-5	James Brakefiel		1751	4		16	57	##	14.7	0.33	1.0	10.7	vhdl	22	Board_cp	min	C,asm	N		64K	64K	Y		5		2003	2012		8080 derivative, optional UART, 8-bit	xilinx 4K RAM primitives
jmr16f84	JMP16F84 PIC M	stable	Julio Rodriguez	PIC16	8	14												1.0		no files						Y							2013		PIC16 data sheets		
or1k	OpenRISC	stable	Julius Baxter, Stefar	OpenRISC	32	32	cyclcon-2	James Brakefiel		3262	4	3	8	68	##	q11.1	1.00	1.0	20.9	verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
or1k	OpenRISC	stable	Julius Baxter, Stefar	OpenRISC	32	32	cyclcon-4	James Br	too many Ios		4				##	q13.1	1.00	1.0		verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
or1k	OpenRISC	stable	Julius Baxter, Stefar	OpenRISC	32	32	arria-2	James Br	failed in fitter		A				##	q13.1	1.00	1.0		verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
or1k	OpenRISC	stable	Julius Baxter, Stefar	OpenRISC	32	32	spartan-3-5	James Br	syntax errors		4				##	14.7	1.00	1.0		verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
or1k	OpenRISC	stable	Julius Baxter, Stefar	OpenRISC	32	32	spartan-6-3	James Brakefiel		3201	6	3	3	77	##	14.7	1.00	1.0	24.1	verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
or1k	OpenRISC	stable	Julius Baxter, Stefar	OpenRISC	32	32	kintex-7-3	James Brakefiel		3299	6	3	3	189	##	14.7	1.00	1.0	57.3	verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU

picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James Brakefiel		178	4			182	##	14.7	0.33	2.0	168.9	vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	kintex-7-3	James Br	ROM paramet		6				##	14.7	0.33	2.0		vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
or1k-cf	Confluence Oper	alpha	Kenr	OpenRISC	32	32														confluence													2004	2009			
gup	HC11 Compatibl	stable	Kevin Phillipson	68HC11	8	8x	arria-2	James Brakefiel		925	A	1	1	127	##	q13.1	0.33	4.0	11.3	vhdl	25	gator_up	yes	yes	N	N	64K	64K	Y				2008	2009	6811 data sheets	68HC11 compatible	top level is schematic
open8_urisc	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakefiel		691	6	1		263	##	14.7	0.33	1.0	125.6	vhdl	9	Open8	yes	yes	N		64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation uRISC processor, in use	
microcore		beta	Klaus Schleisiek	forth	32	8	spartan-6-3	James Brakefiel		591	6		1	71	##	14.7	1.00	1.0	120.1	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/d	AKA uCore110
microcore		beta	Klaus Schleisiek	forth	32	8	kintex-7-3	James Brakefiel		644	6			149	##	14.7	1.00	1.0	231.3	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/d	AKA uCore110
oks8	oks8	alpha	Kongzilee	ARM7	32	32	kintex-7-3	James Br	bad coding pra		6				##	14.7	0.67	1.0		verilog	8	oks8	yes	yes	N		64K	64K	Y				2006	2009		clone of KS86C4204/C4208/P4208, SAM87RI instruction set	
latticemicro8		stable	Lattice Semiconduc	RISC	8	18	LFE2	Lattice Semicon		265	4			104			0.33	2.0	64.4	vhdl	10	isp8_core	yes	yes	N		256	4K	Y		32		2005	2010	en.wikipedia.org/wiki/	16 deep call stack, four configurations	
mips_fault_t	Mips-FaultTolera	stable	Lazaridis	MIPS	32	32												1.0		vhdl			yes	yes	N		4G	4G	Y		32		2013		MIPS data sheets	arithmetic includes fault detection	
mipsr2000	mipsr2000	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakefiel		1971	6	4	6	71	##	14.7	1.00	1.0	36.2	vhdl	35	Dm	yes	yes	N		4G	4G	Y		32	5	2012	2013	MIPS data sheets	course project	
mips_enhanc	MIPS_enhanced	stable	Lazaridis Dimitris, Ic	SPARC	32	32												1.0		vhdl		leon3mp	yes	yes	N		4G	4G	Y		32		2010	2011	tar file does not match	based on mips789, added cache?? Only source is for Leon3	
distributed_i	Distributed limit	planning	Leo Ger		16	16														vhdl	11	mini_uP_x16			N		64K	64K					2009	2009		single stack and 4 data registers	
opencpu32	OpenCPU32	planning	Leonardo Araujo dos Dantos		32	32														vhdl	22	pkgOpenCPU32			N						16		2012	2012		built to test division algorithms	
dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakefiel		788	6			164	##	14.7	0.67	1.0	139.3	vhdl	6	dgf_core	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakefiel		1432	6		1	171	##	14.7	1.00	1.0	119.1	verilog	10	mips_cor	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakefiel		1432	6		1	171	##	14.7	1.00	1.0	119.1	verilog	10	mips_cor	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
lwrisc	ClaiRISC	stable	Li Wu	accum	8	12	arria-2	James Brakefiel		88	A		1	230	##	q13.1	0.17	1.0	443.6	verilog	9	risc_core		asm	N	Y	256	2K	Y	16			2008	2009		simplified PIC, 4 reg rtn stack	absolute addressing only, lowered MIF
neptune-core	The Neptune Co	planning	Llama																	no source													2003	2009		single schematic	
secretblaze		beta	Lyonel Barthe	uBlaze	32	32	spartan-3-4	Lyonel Barthe		1563	4			91		i12.1	1.00	1.0	58.2	vhdl	26	sb_core		yes			4G	4G	Y	86	32	5	2010	2012	www.lirmm.fr/ADAC/		
hmta	HyperMTA	planning	Mahesh Palve	accum	8	16														no files					Y						64		2002	2009		up to 256 threads	
risc_core_i	RISC_Core_I	planning	Manuel Imhof	RISC	16	16	kintex-7-3	James Brakefiel		349	6	1		717	##	14.7	0.67	1.0	1377.2	vhdl	13	CPU	yes	asm	N		1K	1K			8	4	2001	2009		Havard arch	dubious Fmax
or2k	OpenRISC 2000	planning	Marcus Erlandsson etal		32	32														no source																	
dcpu16		beta	Marcus Persson , Sh	RISC	16	16	kintex-7-3	James Brakefiel		662	6	1		318	##	14.7	0.67	4.0	80.4	vhdl & ve	5	dcpu16_	yes	asm	N	N	64K	64K	N	37	8		2009	2012	https://github.com/dc	for the 0X10c game	4+ addressing modes, 4 & 5-bit reg /m
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	Martin Schoebe		189	4		1	160			0.67	1.0	567.2	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3	Martin Schoebe		188	4		1	129			0.67	1.0	459.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin Schoebe		112	6		1	182			0.67	1.0	1088.8	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-2	James Brakefiel		259	4		1	122	##	q11.1	0.67	1.0	316.5	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	James Brakefiel		238	4		1	149	##	q13.1	0.67	1.0	420.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
leros	Leros	stable	Martin Schoeberl	accum	16	16	arria-2	James Brakefiel		164	A		1	266	##	q13.1	0.67	1.0	1086.2	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3-5	James Brakefiel		247	4		1	105	##	14.7	0.67	1.0	285.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	James Brakefiel		174	6		1	155	##	14.7	0.67	1.0	595.9	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
leros	Leros	stable	Martin Schoeberl	accum	16	16	kintex-7-3	James Brakefiel		169	6		1	274	##	14.7	0.67	1.0	1084.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microcon	256 word data RAM, PIC like	short LUT inst ROM
jop	JOP a Java Optim	stable	Martin Schoeberl et	forth	16	16	cyclone-1	Martin Schoebe		2000	4			100		q10.0	0.67	1.0	33.5	vhdl	11	core	yes	yes	N		256K	256K					2004	2014	https://github.com/jop	leros is his later effort	java app builds some source code files
system6801	Wishbone Syster	stable	Michael L. Hasenfra	6801	8	8x	cyclone-3	James Brakefiel		1507	4		3	73	##	14.7	0.33	4.0	4.0	vhdl	15	wb_cyclc	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets	based on John Kent's 6801	tested on Apex20K, Cyclone & Straix b
m16c5x	SoC:M16C5x	mature	Michael Morris	PIC16	8	14	spartan-3-4	Michael Morris		1265	4		3	60	##		0.33	1.0	15.7	verilog	3	m16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets	SOC LUT count	core at P16C5X
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3	Michael Morris		661	4		3	74			0.33	4.0	9.2	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3-5	James Brakefield			4		3		##	14.7	0.33	4.0		verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-6-3	James Brakefiel		466	6		3	118	##	14.7	0.33	4.0	20.8	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
m65c02	M65C02	mature	Michael Morris	6502	8	8x	kintex-7-3	James Brakefiel		661	6		3		##	14.7	0.33	4.0		verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	cyclone-2	James Brakefiel		1216	4			87	##	q11.1	0.33	1.0	23.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	cyclone-4	James Brakefiel		1201	4			102	##	q13.1	0.33	1.0	27.9	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	arria-2	James Brakefiel		649	A			176	##	q13.1	0.33	1.0	89.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-3-5	James Brakefiel		487	4			90	##	14.7	0.33	1.0	60.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-6-3	James Brakefiel		352	6			133	##	14.7	0.33	1.0	124.2	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	kintex-7-3	James Brakefiel		378	6			252	##	14.7	0.33	1.0	220.2	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
synpic12		stable	Miguel Angel Ajo Pe	PIC12	8	12	cyclone-2-6	James Br	ROM	1436	4		1	76	##	q11.1	0.33	1.0	17.5	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCOR
synpic12		stable	Miguel Angel Ajo Pe	PIC12	8	12	cyclone-4-6	James Br	ROM	1417	4		1	96	##	q13.1	0.33	1.0	22.4	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCOR
synpic12		stable	Miguel Angel Ajo Pe	PIC12	8	12	arria-2	James Br	ROM	1098	A			154	##	q13.1	0.33	1.0	46.2	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCOR
synpic12		stable	Miguel Angel Ajo Pe	PIC12	8	12	spartan-3-5	James Brakefiel		805	4		1	58	##	14.7	0.33	1.0	23.8	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCOR
synpic12		stable	Miguel Angel Ajo Pe	PIC12	8	12	spartan-6-3	James Brakefiel		517	6		1	89	##	14.7	0.33	1.0	57.0	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCOR
synpic12		stable	Miguel Angel Ajo Pe	PIC12	8	12	kintex-7-3	James Brakefiel		474	6		1	197	##	14.7	0.33	1.0	136.8	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCOR
risc5x	RISC5x	stable	MikeJ	PIC16	8	14	kintex-7-3	James Br	RLOC constrai		6					14.7	0.33	1.0		vhdl	15	cpu	yes	yes	N	Y	256	4K	Y				2002	2011	PIC16 data sheets	makes extensive use of xilinx primitives	
myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-2	Muza Byt	Altera	186	4		2	57			0.33	1.0	101.2	verilog	1	myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-2	James Brakefiel		182	4		2	93	##	q11.1	0.33	1.0	169.0	verilog	1	myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-4	James Brakefiel		198	4		2	128	##	q13.1	0.33	1.0	212.9	verilog	1	myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	arria-2	James Brakefiel		121	A		2	231	##	q13.1	0.33	1.0	628.7	verilog	1	myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
pepelatz_mis	Pepelatz MISC	planning	Myname IsTeapot	MISC																verilog	1															insignificant source	
m65		stable	Naohiko Shimizu	6502	8	8x	arria-2	James Brakefiel		483	A			110	##	q13.1	0.33	4.0	18.8	sfl & TDF	8	m65cpu	yes	yes	N	N	4K	4K	Y				2001	2002	6502 data sheets		
sparcv8coprc	Coprocessor-rea	planning	Nicholas Voorsange	SPARC	32	32														no files													2012		SPARC data sheets		
avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakefiel		174	6			418	##	14.7	0.33	1.0	792.2	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-2	James Brakefiel		2865	4	1		39	##	q11.1	0.67	2.0	4.6	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-4	James Brakefiel		3252	4			48	##	q13.1	0.67	2.0	4.9	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-5	James Brakefiel		2710	A	1		44	##	q13.1	0.67	2.0	5.4	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	arria-2	James Brakefiel		1966	A	2		77	##	q13.1	0.67	2.0	13.1	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	spartan-3-5	James Brakefiel		2763	4	1		34	##	14.7	0.67	2.0	4.2	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	spartan-6-3	James Brakefiel		2716	6	1		44	##	14.7	0.67	2.0	5.4	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	kintex-7-3	James Brakefiel		2500	6	1		94	##	14.7	0.67	2.0	12.6	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
next186_soc	Next186 SoC PC	stable	Nicolae Dumitrache	8086	16	8x	spartan-3a-	James Br	translate erro		4	1			##	14.7	0.67	2.0		verilog	14	ddr_186	yes	yes	N	N	1M	1M	Y				2013	2014	x86 data sheets	SoC version of next186	boots DOS
next186_soc	Next186 SoC PC	stable	Nicolae Dumitrache	8086	16	8x	kintex-7-3	James Br	translate erro		6	1			##	14.7	0.67	2.0		verilog	14	ddr_186	yes	yes	N	N	1M	1M	Y				2013	2014	x86 data sheets	SoC version of next186	boots DOS

nextz80	NextZ80	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakefiel	1064	6			106	##	14.7	0.33	3.0	10.9	verilog	3	NextZ80	yes	yes	N	N	64K	64K	Y				2011	2014	z80 data sheets		
risc0		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakefiel	1186	6	4	6	110	##	14.7	0.67	1.0	61.9	verilog	8	RISC0	yes	yes	N		4G	4G					2011			minimalist Wirth, education tool	
risc5		beta	Niklaus Wirth	RISC	32	32	cyclone-2	James Brakefiel	3749	4		4	32	##	q11.1	1.00	1.0	8.5	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Obe	32x32 multiplier
risc5		beta	Niklaus Wirth	RISC	32	32	cyclone-4	James Brakefiel	3503	4		1	54	##	q13.1	1.00	1.0	15.4	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Obe	32x32 multiplier ?
risc5		beta	Niklaus Wirth	RISC	32	32	arria-2	James Brakefiel	2362	A		3	73	##	q13.1	1.00	1.0	31.0	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Obe	32x32 multiplier
risc5		beta	Niklaus Wirth	RISC	32	32	spartan-3-5	James Brakefiel	3005	4	4	1	34	##	14.7	1.00	1.0	11.4	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Obe	32x32 multiplier
risc5		beta	Niklaus Wirth	RISC	32	32	spartan-6-3	James Brakefiel	2283	6	4	1	55	##	14.7	1.00	1.0	24.3	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Obe	32x32 multiplier
risc5		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakefiel	2441	6	4	1	92	##	14.7	1.00	1.0	37.8	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Obe	32x32 multiplier
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	arria-2	James Br	expecting a de	A				##	q13.1	0.33	4.0		verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	spartan-3e-	Oleg Odintsov	978	4			50			0.33	4.0	4.2	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	spartan-6-3	James Brakefiel	807	6			80	##	14.7	0.33	4.0	8.2	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	kintex-7-3	James Brakefiel	824	6			176	##	14.7	0.33	4.0	17.7	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	cyclone-4-6	Oliver Girard	1750	4	1		52			0.67	2.0	9.9	verilog	30	openMSI	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver Girard	1147	A	1		98			0.67	2.0	28.5	verilog	30	openMSI	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	spartan-6-4	Oliver Girard	1424	6	1		68			0.67	2.0	15.9	verilog	30	openMSI	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	virtex-6-3	Oliver Girard	1387	6	1		116			0.67	2.0	27.9	verilog	30	openMSI	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-3	Oyvind Harboe	440	4			85			0.10	1.0	19.3	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	opensource.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-6	Oyvind Harboe	1259	6			135			0.10	1.0	10.7	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	opensource.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	kintex-7-3	James Brakefiel	1073	6	3		283	##	14.7	0.10	1.0	26.4	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	opensource.zylin.com	zpu4: 16 & 32 bit versions, code size	zpu4 core
zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	kintex-7-3	James Brakefiel	1352	6	3		276	##	14.7	0.10	1.0	20.4	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	opensource.zylin.com	zpu4: 16 & 32 bit versions, code size	zy2000 core
pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo Kocik	177	4		1	117			0.33	2.0	109.1	verilog	18	pacoblaz	yes	asm	N		256	2K	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	kintex-7-3	James Br	empty project	6					14.7	0.33	2.0		verilog	18	pacoblaz	yes	asm	N		256	2K	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvadeo	48	4			134		q9.1	0.17	1.0	475.9	vhdl	3	usimplez_cpu			N		512	512		8			2011		http://www-gti.det.uv	part of university course, simplez+i4	MIPS/Mhz reduced due to few inst
gumnut		stable	Peter Ashenden	RISC	8	18	cyclone-2	James Brakefiel	3110	4		18	53	##	q11.1	0.33	1.0	5.7	verilog	6	gumnut_	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
gumnut		stable	Peter Ashenden	RISC	8	18	cyclone-4-6	James Brakefiel	3102	4		9	68	##	q13.1	0.33	1.0	7.2	verilog	6	gumnut_	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
gumnut		stable	Peter Ashenden	RISC	8	18	arria-2	James Brakefiel	1264	A		9	120	##	q13.1	0.33	1.0	31.2	verilog	6	gumnut_	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
gumnut		stable	Peter Ashenden	RISC	8	18	spartan-3-5	James Brakefiel	415	4		6	74	##	14.7	0.33	1.0	59.1	verilog	6	gumnut_	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
gumnut		stable	Peter Ashenden	RISC	8	18	spartan-6-3	James Brakefiel	306	6		5	118	##	14.7	0.33	1.0	126.9	verilog	6	gumnut_	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakefiel	305	6		3	185	##	14.7	0.33	1.0	200.4	verilog	6	gumnut_	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakefiel	335	6		3	178	##	14.7	0.33	1.0	175.8	vhdl	20	gumnut_	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakefiel	388	6			259	##	14.7	0.33	1.0	220.7	verilog	6	gumnut-	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakefiel	420	6			275	##	14.7	0.33	1.0	216.2	vhdl	9	gumnut-	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
msl16		beta	Philip Leong, Tsang,	forth	16	4	kintex-7-3	James Brakefiel	303	6			256	##	14.7	0.67	1.0	566.4	vhdl	13	cpu	yes	asm	N		256			16			2001			CPLD prototype	
minimips	miniMIPS	stable	Poppy etal	MIPS	32	32	kintex-7-3	James Brakefiel	2939	6	8		118	##	14.7	1.00	1.0	40.1	vhdl	12	minimips	yes	yes	N		4G	4G	Y		32	5			MIPS I		
or10		simulation	R. Diez	OpenRISC	32	32										1.00	2.0		verilog	6	or10_top	yes	yes	N	M	4G	4G	Y		32		2012	2014		no longer maintained	
minsoc	*minsoc*	stable	Raul Fajardo etal	OpenRISC	32	32	cyclone-2	James Brakefiel	4721	4	4	44	48	##	q11.1	1.00	1.0	10.2	verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
minsoc	*minsoc*	stable	Raul Fajardo etal	OpenRISC	32	32	arria-2	James Br	failed in fitter	A				##	q13.1	1.00	1.0		verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
minsoc	*minsoc*	stable	Raul Fajardo etal	OpenRISC	32	32	spartan-6-3	James Br	too many los	6	4	13		##	14.7	1.00	1.0		verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
minsoc	*minsoc*	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakefiel	4945	6	4	8	107	##	14.7	1.00	1.0	21.7	verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
mcs-4	4004 CPU & MCS	alpha	Reece Pollack	4004	4	4	kintex-7-3	James Brakefiel	228	6			376	##	14.7	0.16	4.0	66.0	verilog	7	i4004			N		4K	4K	N				2012	2012	4004 data sheets	4004 was multi-chip	clks/inst is approx
oc54x	OpenCores54x D	beta	Richard Herveille	DSP	16	16	kintex-7-3	James Brakefiel	2225	6	1		180	##	14.7	0.67	1.0	54.1	verilog	10	oc54_cpu	yes	yes	N	Y	64K	64K					2002	2009		40-bit accumulator, barrel shifter	C54x clone
8bit_chapman		beta	Rob Chapman, Stev	forth	8	8	kintex-7-3	James Br	syntax errors	6					14.7	0.33	1.0		vhdl	10	top	yes		N		256	256					1998			course work	
dataflow_chapman		alpha	Rob Chapman, Stev	forth			kintex-7-3	James Br	file WebCase	6					14.7	0.33	1.0		vhdl	27	DataFlow	yes		N		256	256					2003			course work	
klc32	KLC32	planning	Robert Finch	RISC	32	32													verilog	25	KLC32	yes		N		4G	4G	Y		32		2011	2012			
raptor64	Raptor64	planning	Robert Finch	RISC	64	32	kintex-7-3	James Br	missing port n	6					14.7	1.50	1.0		verilog	48	Raptor64	yes	yes	Y		2<<64	2<<64	Y		32		2012	2013		8-16-32-64 bit data, cache, MMU, hyper-threaded version also	
rtf65002	RTF65002	alpha	Robert Finch	accum	32	8x	kintex-7-3	James Brakefiel	13615	6	4	4	78	##	14.7	0.67	2.0	1.9	verilog	10	rtf65002	yes		N		4G	4G	Y		16		2013	2013		32-bit 6502 + 6502 emulation	"proven"
rtf65002	RTF65002	alpha	Robert Finch	accum	32	8x	kintex-7-3	James Brakefiel	11216	6	4	6	111	##	v14.1	0.67	2.0	3.3	verilog	10	rtf65002	yes		N		4G	4G	Y		16		2013	2013		32-bit 6502 + 6502 emulation	"proven"
rtf68ksys	rtf68kSys	alpha	Robert Finch	68000	16	16x	spartan-3e-	James Br	need	13639	4	12	17		##	14.7	0.67	4.0		verilog	49	rtf68kSys	yes	yes	N	N	4G	4G	Y		16		2011	2011	68000 data sheets	based on Tobias Gubener's TG68	
rtf8088	rtf8088	planning	Robert Finch	8086	8x	8x	kintex-7-3	James Brakefiel	4514	6	4		174	##	14.7	0.67	3.0	8.6	verilog	57	rtf8088	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	8-bit memory data, e.g. 8088	
ssbcc	Smal Stack Base	stable	Rodney Sinclair	forth	8	9	arria-2	James Br	syntax errors	A				##	q13.1	0.33	1.0		system ve	3	core	yes	asm	N				Y				2012	2014		Python program generates the Verilog	
dfp	dfp	stable	Ron Chapman	forth	8	Y	spartan-6-3	James Brakefiel	334	6			112	##	14.7	0.33	1.0	110.7	vhdl	25	DataFlow	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
dfp	dfp	stable	Ron Chapman	forth	8	Y	kintex-7-3	James Brakefiel	297	6			192	##	14.7	0.33	1.0	213.2	vhdl	25	DataFlow	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	cyclone-3	James Brakefiel	2831	4		22	82	##	q13.1	0.33	3.0	3.2	vhdl	19	top_de1	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	removed pin assignments
z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	spartan-3e-	James Brakefiel	2474	4	2	19	78	##	14.7	0.33	3.0	3.4	vhdl	19	top_s3e	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	
minirisc	Mini-Risc core	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf Usselma	460	4			80			0.33	1.0	57.4	verilog	7	risc_core	yes	yes	N	Y	256	4K	Y				2001	2012	PIC16 data sheets		
avr_core	avr_core	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James Brakefiel	2135	6			127	##	14.7	0.33	1.0	19.7	verilog	15	avr_core	yes	yes	N		64K	128K	Y		32		2002	2012	AVR data sheets	VHDL core included	
ecpu	ecpu	planning	Sahrfili Matturi																verilog												2009	2009			
sxp	SXP (Simple eXte	beta	Sam Gladstone etal	RISC	32	32			too many los										verilog		sxp			N		4G	4G			32		2001	2009		basic RISC	too many Ios
manik		stable	Sandeeo Dytta	RISC	32	32	kintex-7-3	James Br	needs editing	6					14.7	0.33	1.0		vhdl	45	manik2tc	yes	yes	N		4K	4K	Y		16		2002	2006	www.niktech.com/	optional data & inst caches	supports Xilinx, Altera, Actel, Lattice
cpu8080	8080 Compativle	stable	Scott Moore	8080	8	8x	spartan-6-3	James Brakefiel	1269	6			129	##	14.7	0.33	9.0	3.7	verilog	1	m8080	yes	yes	N	N	64K	64K	Y				2006	2009	8080 data sheets	includes VGA display generator, three variants	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	cyclone-2	James Brakefiel	1567	4			74	##	q11.1	0.33	1.0	15.6	verilog	1	softusb_	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	cyclone-4-6	James Brakefiel	1561	4			102	##	q13.1	0.33	1.0	21.5	verilog	1	softusb_	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	cyclone-5	James Brakefiel	1566	A			103	##	q13.1	0.33	1.0	21.8	verilog	1	softusb_	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	arria-2	James Brakefiel	1126	A			154	##	q13.1	0.33	1.0	45.1	verilog	1	softusb_	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	spartan-3-5	James Br	internal error	4				##	14.7	0.33	1.0		verilog	1	softusb_	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	spartan-6-3	James Brakefiel	1038	6			116	##	14.7	0.33	1.0	36.9	verilog	1	softusb_	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	kintex-7-3	James Brakefiel	990	6			207	##	14.7	0.33	1.0	69.0	verilog	1	softusb_	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
navre	Navre AVR clone	stable	Sebastien Bourdeau	AVR	8	16	ecp-3-6	James Brakefiel	1338	4			40	##	3.1	0.33	1.0	9.8	verilog	1	softusb_	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
y80e	Y80e Z80/Z180 c	stable	Sergey Belyashov	Z80	8	8x	kintex-7-3	James Br	empty project	6					14.7	1.00	3.0		verilog	15	y80_top	yes	yes	N	N	64K	64K	Y				2013	2013	z80 data sheets	based on Y80 from "Microprocessor Design Using Verilog HDL" by Monte Da	
erp	Educational RISC	stable	Shahzadjk	RISC	8	16	spartan-3-5	James Brakefiel	366	4	1	1	70	##	14.7	0.33	1.0	63.5	verilog	1	ERPveril	yes							15	6		2004	2009		two report PDFs & one Verilog file	

erp	Educational RISC	stable	Shahzadjk	RISC	8	16	kintex-7-3	James Br	4K primitives		6				##	14.7	0.33	1.0		verilog	1	ERPverilog	yes							15	6		2004	2009		two report PDFs & one Verilog file	
ae18	ae18	beta	Shawn Tan	PIC18	16	24	cyclone-2	James Brakefiel		1395	4	1	1	133	##	q11.1	0.67	1.0	63.7	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	cyclone-4-6	James Brakefiel		1505	4		1	144	##	q13.1	0.67	1.0	64.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James Brakefiel		1084	A	1		207	##	q13.1	0.67	1.0	128.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	spartan-6-3	James Brakefiel		1176	6	1		81	##	14.7	0.67	1.0	46.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	virtex-6-3	James Brakefiel		1133	6	1		117	##	14.7	0.67	1.0	69.1	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
ae18	ae18	beta	Shawn Tan	PIC18	16	24	kintex-7-3	James Brakefiel		1131	6	1		68	##	14.7	0.67	1.0	40.5	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	cyclone-2	James Brakefiel		1605	4	3	4	74	##	q11.1	1.00	1.0	46.2	verilog	7	aeMB_cc	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	cyclone-4-6	James Brakefiel		2286	4		4	68	##	q13.1	1.00	1.0	29.5	verilog	7	aeMB_cc	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	arria-2	James Brakefiel		1078	A	4	4	104	##	q13.1	1.00	1.0	96.1	verilog	7	aeMB_cc	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	spartan-3e-	James Brakefiel		1514	4	3	3	54	##	i14.7	1.00	1.0	35.5	verilog	7	aeMB_cc	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	spartan-6-3	James Brakefiel		1053	6	3		71	##	i14.7	1.00	1.0	67.3	verilog	7	aeMB_cc	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakefiel		1018	6	3		131	##	14.7	1.00	1.0	128.5	verilog	7	aeMB_cc	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
k68	K68	alpha	Shawn Tan	68000	8	16x	kintex-7-3	James Brakefiel		2392	6			24	##	14.7	0.67	4.0	1.7	verilog	15	k68_cpu	yes	yes	N	N	4K	4G	Y		16		2003	2009	68000 data sheets	68K binary compatible	
x32		stable	Sijmen Woutersen	forth	32	8	kintex-7-3	James Br	missing define		6				##	14.7	1.00	1.0		vhdl	32	core	yes	yes	N		4G	4G	Y				2006	2007		MS thesis, byte code, needs caches	
8051	8051	alpha	Simon Teran, Jakas	8051	8	8	spartan-3a-	James Br	missing modu		4				##	14.7	0.80	1.0		verilog	32	oc8051_t	yes	yes	N		64K	64K	Y				2001	2013	8051 data sheets		
aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	arria-2	James Br	xilinx primitive		A				##	q13.1	1.00	1.0		verilog	10	DLX_top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakefiel		3586	6			257	##	14.7	1.00	1.0	71.7	verilog	10	DLX_top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
bobcat		beta	Stan Drey		16	24	kintex-7-3	James Brakefiel		1622	6	1		107	##	14.7	0.67	1.0	44.0	vhdl							64K	64K					1998			appears to be a DSP	
wb4pb	Software Aided \	stable	Stefan Fischer	picoBlaze	13	13														vhdl & ve	10					Y							2010	2013	picoblaze data sheets	software addon for picoBlaze	
ncore	nCore	alpha	Stefan Istvan	RISC	8	8														verilog	3	nCore	yes		N					16	16		2006	2009			
atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-3a-	Stephan Nolting		2406	4	1	11	81	##	14.7	0.80	1.0	27.0	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	cyclone-4-6	Stephan Nolting		2967	4	1	32	99	##	q13.1	0.80	1.0	26.7	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	cyclone-2	James Brakefiel		2711	4	1	74	71	##	q11.1	0.80	1.0	21.0	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakefiel		1624	A	2	32	118	##	q13.1	0.80	1.0	58.3	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-3a-	James Brakefiel		2450	4	1	9	76	##	14.7	0.80	1.0	24.9	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-6-3	James Brakefiel		1545	6	1	10	100	##	14.7	0.80	1.0	51.5	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakefiel		1512	6	1	5	149	##	14.7	0.80	1.0	79.1	vhdl	19	ATLAS_2	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakefiel		810	A	2	0	123	##	q13.1	0.80	1.0	121.2	vhdl	8	ATLAS_C	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-6	James Brakefiel		643	6	1	0	103	##	14.7	0.80	1.0	127.9	vhdl	8	ATLAS_C	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakefiel		648	6	1	0	168	##	14.7	0.80	1.0	207.6	vhdl	8	ATLAS_C	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakefiel		559	6	1	0	200	##	v14.1	0.80	1.0	286.2	vhdl	8	ATLAS_C	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	cyclone-2-6	Stephan Nolting		11469	4	3	75	179			1.00	1.0	15.6	vhdl	16	STORM_	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	cyclone-4-6	Stephan Nolting		11518	4	3	67	157			1.00	1.0	13.7	vhdl	16	STORM_	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakefiel		2312	6	3		179	##	14.7	1.00	1.0	77.4	vhdl	16	CORE	yes	yes	N		4G	4G	Y		32	8	2011	2014		I & D caches not compiled	
storm_core	Storm Core (ARM	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakefiel		3514	6	3	4	157	##	14.7	1.00	1.0	44.8	vhdl	16	STORM_	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
plasma	Plasma most MI	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakefiel		2462	6		3	97	##	14.7	1.00	1.0	39.5	vhdl	22	plasma	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	wide outside use, opencores page has list of related publications	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	1 slot	1199	6			127	##	14.7	0.33	1.0	35.0	vhdl	9	avr_core	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	2 slot	1554	6			223	##	14.7	0.33	1.0	47.4	vhdl	10	avr_core	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	3 slot	1812	6			243	##	14.7	0.33	1.0	44.2	vhdl	10	avr_core	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James Br	4 slot	2054	6			278	##	14.7	0.33	1.0	44.7	vhdl	10	avr_core	som	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
cortex_m3	cortex_m3	?	Strauch Tobias	ARM c3	32	16														no files													2013		cortex M3 data sheets	claims to be mature	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauch T	1 slot	3663	6			72	##		1.00	1.0	19.7	verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		original version of OR1200	numbers from published paper
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauch T	2 slot	4535	6			136	##		1.00	1.0	30.1	verilog	39	or1200_t	yes	yes	Y		4G	4G	Y		32		2010	2013		2 slot barrel version of OR1200	numbers from published paper
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauch T	3 slot	5602	6			185	##		1.00	1.0	33.1	verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		3 slot barrel version of OR1200	numbers from published paper
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauch T	4 slot	6286	6			204	##		1.00	1.0	32.5	verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		4 slot barrel version of OR1200	numbers from published paper
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Br	1 slot barrel		6					14.7	1.00	1.0		verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		original version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Br	2 slot translat		6				##	14.7	1.00	1.0		verilog	39	or1200_t	yes	yes	Y		4G	4G	Y		32		2010	2013		2 slot barrel version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Br	3 slot barrel		6					14.7	1.00	1.0		verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		3 slot barrel version of OR1200	
or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James Br	4 slot barrel		6					14.7	1.00	1.0		verilog	39	or1200_i	yes	yes	Y		4G	4G	Y		32		2010	2013		4 slot barrel version of OR1200	
cqpic		stable	Sumio Morioka	PIC16	8	14	arria-2	James Br	ROM paramet		A				##	q13.1	0.67	1.0		vhdl & ve	5	CQPIC	yes	yes	N	Y	256	4K	Y				1999	2004	PIC16 data sheets	LPM macros	http://www002.upp.so-net.ne.jp/mor
jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakefiel		723	6			178	##	14.7	0.33	1.0	81.4	vhdl	3	Processo	yes							27	16		2002			neural network microprocessor, specialized registers	
ARC		proprietar	Synopsys		32	16												1.0		not avail							4G	4G								range of reduced SPARC? uP	
eight_bit_uc		stable	Synplicity	RISC	8	12	kintex-7-3	James Br	signal/variable		6					14.7	0.67	1.0		vhdl	10	eight_bit_uc						2K	Y		32					part of Amplify documentation	
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	arria-2	James Brakefiel		4888	A	2	1	162	##	q13.1	0.67	2.0	11.1	vhdl	3	cpu	yes	yes	Y	N	64K	64K			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	arria-2	James Brakefiel		13221	A	2	14	35	##	q13.1	0.67	2.0	0.9	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James Brakefiel		5060	6	1		205	##	14.7	0.67	2.0	13.6	vhdl	3	cpu	yes	yes	Y	N	64K	64K			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James Brakefiel		13495	6	1	3	6	##	14.7	0.67	2.0	0.2	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/
pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James Brakefiel		13327	6	1		45	##	v14.1	0.67	2.0	1.1	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/
yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	arria-2	James Br	map errors		A				##	q13.1	1.00	1.0		verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntations	
yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James Br	map e	2220	6	6			##	14.7	1.00	1.0		verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntations	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	cyclone-2	James Brakefiel		1250	4		3	88	##	q11.1	1.00	1.0	70.8	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheet	not all instructions implemented	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	cyclone-4	James Brakefiel		1255	4		3	115	##	q13.1	1.00	1.0	91.4	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheet	not all instructions implemented	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	arria-2	James Brakefiel		784	A		3	183	##	q13.1	1.00	1.0	232.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheet	not all instructions implemented	
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	spartan-3-5	James Brakefiel		1367	4		3	80	##	14.7	1.00	1.0	58.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheet	not all instructions implemented	moved everything to work library
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	spartan-6-3	James Brakefiel		911	6		2	114	##	14.7	1.00	1.0	125.3	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheet	not all instructions implemented	moved everything to work library
mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	kintex-7-3	James Brakefiel		941	6		2	227	##	14.7	1.00	1.0	240.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data sheet	not all instructions implemented	moved everything to work library
cowgirl	Cowgirl	beta	Thebeekeeper		16	16	kintex-7-3	James Br	empty design		6					14.7	0.67	1.0		vhdl	14	cowgirl						64K					2006	2009			
free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakefiel		355	6			142	##	14.7	0.33	1.0	132.2	verilog	8	cpu	yes	yes	N		256	4K	Y				2002	2011	PIC16 data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	cyclone-2	James Brakefiel		5237	4	2	32	33	##	q11.1	1.00	1.0	6.3	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		

aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	cyclone-4-6	James Brakefiel		6034	4		32	43	##	q13.1	1.00	1.0	7.2	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	arria-2	James Brakefiel		3209	A	4	32	70	##	q13.1	1.00	1.0	22.0	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	spartan-3-5	James Brakefiel		5618	4	2	32	31	##	14.7	1.00	1.0	5.5	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	spartan-6-3	James Brakefiel		4180	6	2	12	49	##	14.7	1.00	1.0	11.8	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakefiel		4071	6	2	10	97	##	14.7	1.00	1.0	23.7	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James Brakefiel		41	6			384	##	14.7	0.08	1.0	749.0	vhdl	1	tb02cpu2	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
tg68	TG68 execute 68	stable	Tobias Gubener	68000	16	16x	kintex-7-3	James Brakefiel		2331	6			44	##	14.7	0.67	4.0	3.2	vhdl	2	TG68_fas	yes	yes	N	N	4G	4G	Y		16		2007	2012	68000 data sheets	for use with Minimig	
pic_coonan		alpha	Tom Coonan	PIC16	8	14	kintex-7-3	James Brakefiel		328	6		1	165	##	14.7	0.33	1.0	166.1	verilog	7	piccpu	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets		
cf_ssp	CF State Space P	stable	Tom Hawkins	?																confluence													2003	2009		confluence to VHDL	
fpgammix		stable	Tommy Thorn	MMIX	64	32	arria-2	James Brakefiel		11605	A	8	10	94	##	q13.1	1.50	4.0	3.0	system ve	2	core	yes	yes	Y	Y	4G	4G	Y	256	288		2006	2008		clone of Knuth's MMIX	micro-coded
fpgammix		stable	Tommy Thorn	MMIX	64	32	kintex-7-3	James Br	unacceptable		6				##	14.7	1.50	4.0		system ve	2	core	yes	yes	Y	Y	4G	4G	Y	256	288		2006	2008		clone of Knuth's MMIX	micro-coded
dalton_8051		stable	Tony Givargis	8051	8	8x	kintex-7-3	James Brakefiel		2725	6	1	1	105	##	14.7	0.33	1.0	12.7	vhdl	7	i8051_all	yes	yes	N	N	64K	64K	Y				1999	2003	8051 data sheets	ASIC	www.cs.ucr.edu/~dalton/
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-3-5	James Brakefiel		1937	4	1	3	20	##	14.7	0.33	4.0	0.9	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James Brakefiel		1412	6	1	3	31	##	14.7	0.33	4.0	1.8	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
ic6821	vhdl core of IC68	beta	Ttsenis		8													1.0		vhdl	1	VHDL682	yes										2005	2009	6800 data sheets	VHDL for M6821	
68hc05	68hc05	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James Brakefiel		1225	6			300	##	14.7	0.33	4.0	20.2	vhdl	1	6805		yes	N	N	64K	64K	Y				2007	2009	6805 data sheets		
68hc08	68hc08	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James Brakefiel		2290	6			101	##	14.7	0.33	4.0	3.6	vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009	6808 data sheets		
tiny64	Tiny64	stable	Ulrich Riedel	RISC	64		kintex-7-3	James Br	bit length mis		6					14.7	1.00	1.0		vhdl	7	TinyX		asm	N		64K	64K		16	8		2004	2009		word size configurable from 32 to 64	
tiny8	tiny8	mature	Ulrich Riedel	CISC	8	8x			Flex10K design									1.0		ahdl & schematic				asm	N		64K	64K	Y				2002	2009		registers in RAM like TMS9900, uses Altera AHDL, megafunctions & schemat	
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	cyclone-2	James Brakefiel		3952	4		33	67	##	q11.1	1.00	1.0	16.9	system ve	17	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	cyclone-4-6	James Brakefiel		3874	4		17	81	##	q13.1	1.00	1.0	21.0	system ve	17	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	arria-2	James Brakefiel		2346	A		6	141	##	q13.1	1.00	1.0	60.1	system ve	17	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	spartan-3e-	James Br	declar	3897	4		9	61	##	i14.7	1.00	1.0	15.6	system ve	16	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	xilinx S3 primitives
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	spartan-6-3	James Brakefiel		2546	6		9	91	##	i14.7	1.00	1.0	35.9	system ve	16	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	xilinx S3 primitives
altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James Brakefiel		2602	6		5	176	##	i14.7	1.00	1.0	67.5	system ve	16	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	xilinx S3 primitives
altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	cyclone-2	James Brakefiel		3144	4			87	##	q11.1	1.00	2.0	13.8	system ve	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipelin	LPMs & systemVerilog
altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	cyclone-4-6	James Brakefiel		3002	4			88	##	q13.1	1.00	2.0	14.6	system ve	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipelin	LPMs & systemVerilog
altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	arria-2	James Brakefiel		1815	A			163	##	q13.1	1.00	2.0	44.9	system ve	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipelin	LPMs & systemVerilog
altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	spartan-3e-	James Brakefiel		2689	4			75	##	i14.7	1.00	2.0	14.0	system ve	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipelin	xilinx S3 primitives
altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	spartan-6-3	James Brakefiel		1837	6			115	##	i14.7	1.00	2.0	31.4	system ve	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipelin	xilinx S3 primitives
altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James Brakefiel		1928	6			236	##	i14.7	1.00	2.0	61.3	system ve	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipelin	xilinx S3 primitives
mpx	MPX 32-bit CPU	stable	Ultra Embedded		32	32														verilog					N		4G	4G	Y		32		2012	2013		GCC tools, no Verilog	
hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakefiel		875	6			136	##	14.7	0.67	1.0	104.2	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
qrisc32	qrisc32 wishbon	alpha	Viacheslav	RISC	32	32	arria-2	James Brakefiel		3075	A	4		144	##	q13.1	1.00	1.0	46.9	system ve	8	qrisc32	yes	yes	N		4G	4G	Y		32	4	2010	2011		for PhD thesis	
tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	spartan-6-3	James Brakefiel		198	6			60	##	14.7	0.33	1.0	99.5	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
tisc	Tiny Instruction	beta	Vincent Crabtree	accum	8	8x	kintex-7-3	James Brakefiel		195	6			87	##	14.7	0.33	1.0	147.1	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
w11	PDP-11/70 CPU	alpha	Walter Mueller	PDP11	8	16x	spartan-6	Walter Mueller		3418	6			80			0.67	2.0	7.8	vhdl	26	pdp11	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
w11	PDP-11/70 CPU	alpha	Walter Mueller	PDP11	8	16x	kintex-7-3	James Brakefiel		1760	6	1	1	147	##	14.7	0.67	2.0	28.0	vhdl	118	pdp11_c	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
w11	PDP-11/70 CPU	alpha	Walter Mueller	PDP11	8	16x	kintex-7-3	James Brakefiel		3174	6	1	3	131	##	14.7	0.67	2.0	13.9	vhdl	133	sys_w11a	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
ucore	Ucore	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakefiel		2469	6		1	231	##	14.7	1.00	1.0	93.5	verilog	25	ucore	yes	yes	N		4G	4G	Y		32	6	2005	2010	MIPS data sheets	MMU & caches	
socz80		stable	Will Sowerbutts	Z80	8	8x	spartan-6-3	James Br	constr	2568	6		15	93	##	14.7	0.33	3.0	4.0	vhdl	25	top_level	yes	yes	N	N	64K	64K	Y				2013	2014	z80 data sheets	based on Daniel Wallner's T80, for Pa	http://sowerbutts.com/socz80/
socz80		stable	Will Sowerbutts	Z80	8	8x	kintex-7-3	James Br	source uses Sp		6		8		##	14.7	0.33	3.0		vhdl	25	top_level	yes	yes	N	N	64K	64K	Y				2013	2014	z80 data sheets	based on Daniel Wallner's T80, for Pa	http://sowerbutts.com/socz80/
suska-III		beta	Wolfgang Forster	68000	16	16x	cyclone-4-6	James Brakefiel		9894	4			34	##	q13.1	0.67	4.0	0.6	vhdl	11	wf68k00i	yes	yes	N	N	4G	4G	Y		16		2003	2013	68000 data sheets	for use as an Atari ST	http://www.experiment-s.de/en/
suska-III		beta	Wolfgang Forster	68000	16	16x	arria-2	James Brakefiel		7388	A			55	##	q13.1	0.67	4.0	1.3	vhdl	11	wf68k00i	yes	yes	N	N	4G	4G	Y		16		2003	2013	68000 data sheets	for use as an Atari ST	http://www.experiment-s.de/en/
lemberg		stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4-6	James Brakefiel		37459	4	25	54	43	##	q13.1	1.00	1.0	1.1	vhdl	57	core	yes	yes	Y		4G	2M	Y		32	4	2011		www2.imm.dtu.dk/~w	upto 4 inst/clock	LPM mem & floating point
lemberg		stable	Wolfgang Puffitsch	VLIW	32	32	arria-2	James Br	failed in fitter		A				##	q13.1	1.00	1.0		vhdl	57	core	yes	yes	Y		4G	2M	Y		32	4	2011		www2.imm.dtu.dk/~w	upto 4 inst/clock	LPM mem & floating point
marca	McAdam's RISC	stable	Wolfgang Puffitsch	RISC	16	16	arria-2	James Brakefiel		1763	A		22	157	##	q13.1	0.67	6.0	10.0	vhdl	40	marca	yes		N		8K	16K		75	16	4	2007	2009		serial multiply & divide	clks/inst is approx
microblaze		proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		1201	6		32	408			1.30	1.0	441.4	not avail			yes	yes	opt		4G	4G	Y	86	32	5	2002		www.xilinx.com/tools/	performance optimized	70 configuration options, MMU option
microblaze		proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546	6		1	320			1.03	1.0	603.7	not avail			yes	yes	opt		4G	4G	Y	86	32	3	2002		www.xilinx.com/tools/	MicroBlaze MCS, smallest configurati	70 configuration options, MMU option
yasep		alpha	Yann Guidon	RISC	16	32	kintex-7-3	James Br	syntax errors		6					14.7	1.00	1.0		vhdl		microYAE	yes	asm	N			2K			16		2008	2014	www.yaesp.org	Java generated VHDL, revisions ongo	funky web site
latticemicro32		stable	Yann Siommeau, M	RISC	32	32	arria_2	James Brakefiel		2166	A	4	30	149	##	q13.1	0.80	1.0	55.0	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki/	optional data & inst caches	
latticemicro32		stable	Yann Siommeau, M	RISC	32	32	spartan-6	James Brakefiel		2093	6	3	15	85	##	14.7	0.80	1.0	32.4	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki/	optional data & inst caches	
latticemicro32		stable	Yann Siommeau, M	RISC	32	32	kintex-7-3	James Brakefiel		2292	6	3	8	155	##	14.7	0.80	1.0	54.2	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki/	optional data & inst caches	
pdp1	PDP-1 reimplem	alpha	Yann Vernier	PDP1	18	18	spartan-3a-	James Brakefiel		1390	4		6	138	##	14.7	0.50	10.0	5.0	vhdl		top	yes	yes	N	N	4K	4K		28			2011	2011	http://pdp-1.compute	PDP-1 descended from MIT TX-0	uses Minimal UART from opencores
riscmcu	RISC Microcontr	stable	Yapzihe	AVR	8	16	arria-2	James Br	LPM paramet		6					14.7	0.33	1.0		vhdl	15	v_riscmc	yes	yes	N		128	512	Y	92	16		2002	2009	AVR data sheets		
zet86	Zet The x86 (IA-3	alpha	Zeus Marmolejo	8086	16	8x	kintex-7-3	James Brakefiel		3642	6	1		68	##	14.7	0.67	2.0	6.2	verilog	32	fpga_zet	yes	yes	N	N	1M	1M	Y				2008	2014	x86 data sheets	equivalent to 80186, boots MS-DOS	zet.aluzina.org/index.php/Zet_process
inst_list_proc	8-bit Pipelined P	planning					kintex-7-3	James Brakefield			6				##	14.7	0.33	1.0		verilog	34	top	yes		N								2014				
mproz		stable		RISC	16	16														schematic			yes	asm	N			32K					1999			little documentation, CPLD implementation	
totalcpu	TotalCPU	alpha		RISC	12+	12														verilog											16		2007	2009		data width 12 bits and up, no data memory	

126 # usable(beta, stable or mature): "A"(clones) & "W"(originals) 51 ⌗ ⌗ ⌗

65 "B" or "X" of limited interest **171 unique usable designs**

\# adrs

Web page DMIPS per clock cycle per core en.wikipedia.org/wiki/Instructions_pe community.freescale.c www.eembc.org/coremark/index.php

MIPS/MHz Pro-rating for data size:

1-bit	0.04		
8-bit	0.33	**Silicon Area equivalents**	
16-bit	0.67	LUTS/DSP48	16:1
32-bit	1.00	LUTS/Block RAM	32:1

Under the assumption that the core is capable of one instuction per clock

Following has DMIPS per clock for many microprocessors
http://en.wikipedia.org/wiki/Instructions_per_second

uP	MIPS		CoreMarks /MHz	MHz	guessed average clocks/inst
4004	0.10				
6502	0.50		0.02	0.06	4
8051	0	DMIPS	0.08	0.24	1, 4 or 6
8080	0.17			0.25	9
68K	0.10			0.15	4

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	used to indicate best KIPS/LUT for a given design, usually using fast FPGA family
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing, usually using fastest part grade
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALUT	4-LUT, 6-LUT, Altera ALUT, Actel Tile
LUT?	total number of LUTs or ALUTs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up
blk RAM	total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up
Fmax	maximum primary clock speed from compile, place & route run without clock constraints
date	date of compile, place & route; serves to identify source version
tool ver	Altera (**Q**uartus), Xilinx (ISE, **V**ivado), Lattice Semiconductor(**D**iamond) or MicroSemi(**L**ibero) tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or System Verilog or schematic or gates
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall

ARM Cortex A9	2.50	DMIPS		2.90	1000		
ARM Cortex M0	0.90	DMIPS		1.50	70		
ARM Cortex M3	1.25	DMIPS		2.17	25		
ARM7	0.90		0.74	2.04	600		
AVR	1.00		0.21	0.53	8		
AVR32				1.62	60		
BA21				2.44	400		
Coldfire				2.80	400		
Coldfire				0.77	150	Virtex-5	2
HCS08			0.04	0.12			4
HC11							4
LEON3/Spartan-6				1.96	100		
MC6809	1.24		0.07	1.86			3
MicroBlaze 3-stage	1.03			1.50			
MicroBlaze 5-stage	1.38			1.90	125		
MIPS32	1.51			2.28			
MSP430			0.40	1.20			2
MSP430				1.10	25		2
Nios II	0.64	DMIPS		0.93	200		
Nios II -e	0.15	DMIPS		0.25			
Nios II -f	1.13	DMIPS		1.60	200		
PIC16	0.25						
PIC18				0.04	40		
PIC24			0.72	1.86	40		
PIC32				3.45	80		
Super H-2				1.44	180		
VAX780	1.00	DMIPS		1.50		DMIPS # is by definition	
Z80	1.60		0.01	0.03			3
eSi-1600				1.98			