Opencore and other soft core processors

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
		1664	1664 microproce	sim?	Denis Godinho																	C									26			2010	2010		C based simulation only	
X		4stack		simulation	Bernd Paysan	forth	32	5	kintex-7-3	James	source errors	6				##	14.7	0.67	1.0		verilog	80	4stack	yes	yes	Y								2002	2011	bernd-paysan.de/b16.html		
		6502_verilog	6502_verilog_de	sim?	Hyungok Tak	6502	8	8x														verilog				yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	no files, simulated	
		6502vhdl	6502vhdl	planning	Huyvo	6502	8	8x														C				yes	N	N	64K	64K	Y				2003	2009	6502 data sheets	to have a C program generate VHDL	
A		6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8	8x	spartan-6-3	James	Brakef	2061	6			109	##	14.7	0.33	3.0	5.8	verilog	5	MC6809_cpu		yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
A	1	6809_6309	6809_6309_com	beta	Alejandro Paz Schmidt	6809	8	8x	kintex-7-3	James	Brakef	2207	6			212	##	14.7	0.33	3.0	10.6	verilog	5	MC6809_cpu		yes	N	N	64K	64K	Y				2012	2013	6809 data sheets	includes 6309 op-codes, xilinx & lattice projects	
B	1	68hc05	68hc05	stable	Ulrich Riedel	6805	8	8x	kintex-7-3	James	Brakef	1225	6			300	##	14.7	0.33	4.0	20.2	vhdl	1	6805		yes	N	N	64K	64K	Y				2007	2009	6805 data sheets		
B	1	68hc08	68hc08	stable	Ulrich Riedel	6808	8	8x	kintex-7-3	James	Brakef	2290	6			101	##	14.7	0.33	4.0	3.6	vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009	6808 data sheets		
		8051	8051	alpha	Simon Teran, Jakas	8051	8	8	spartan-3a-	James	missing modu	4				##	14.7	0.80	1.0		verilog	32	oc8051_t	yes	yes	N		64K	64K	Y				2001	2013	8051 data sheets		
X		8bit_chapman		beta	Rob Chapman, Steven	forth	8	8	kintex-7-3	James	syntax errors	6					14.7	0.33	1.0		vhdl	10	top	yes		N		256	256					1998		course work		
A		ae18	ae18	beta	Shawn Tan	PIC18	16	24	cyclone-2	James	Brakef	1395	4	1	1	133	##	q11.1	0.67	1.0	63.7	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A		ae18	ae18	beta	Shawn Tan	PIC18	16	24	cyclone-4-6	James	Brakef	1505	4		1	144	##	q13.1	0.67	1.0	64.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A	1	ae18	ae18	beta	Shawn Tan	PIC18	16	24	arria-2	James	Brakef	1084	A	1		207	##	q13.1	0.67	1.0	128.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A		ae18	ae18	beta	Shawn Tan	PIC18	16	24	spartan-6-3	James	Brakef	1176	6	1		81	##	14.7	0.67	1.0	46.2	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A		ae18	ae18	beta	Shawn Tan	PIC18	16	24	virtex-6-3	James	Brakef	1133	6	1		117	##	14.7	0.67	1.0	69.1	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A		ae18	ae18	beta	Shawn Tan	PIC18	16	24	kintex-7-3	James	Brakef	1131	6	1		68	##	14.7	0.67	1.0	40.5	verilog	1	ae18_core		yes	N	Y	4K	1M					2003	2009	PIC18 data sheets	not 100% compatable	negative edge reset "clock"
A		aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	cyclone-2	James	Brakef	1605	4	3	4	74	##	q11.1	1.00	1.0	46.2	verilog	7	aeMB_co	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
A		aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	cyclone-4-6	James	Brakef	2286	4		4	68	##	q13.1	1.00	1.0	29.5	verilog	7	aeMB_co	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
A		aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	arria-2	James	Brakef	1078	A	4	4	104	##	q13.1	1.00	1.0	96.1	verilog	7	aeMB_co	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
A		aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	spartan-3e-	James	Brakef	1514	4	3	3	54	##	i14.7	1.00	1.0	35.5	verilog	7	aeMB_co	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
A		aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	spartan-6-3	James	Brakef	1053	6	3		71	##	i14.7	1.00	1.0	67.3	verilog	7	aeMB_co	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
A	1	aeMB	aeMB	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James	Brakef	1018	6	3		131	##	14.7	1.00	1.0	128.5	verilog	7	aeMB_co	yes	yes	N		4G	4G	Y				2004	2009	xilinx documentation	not 100% compatable	
		af65k		alpha	Andre Fachat	6502	16	8x	kintex-7-3	James	syntax errors	6				##	14.7	0.67	4.0		vhdl			yes		N	N							2011			extended 6502 with 16, 32 or 64 bit data	
		ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	arria-2	James	expecting a de	A				##	q13.1	0.33	4.0		verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
A		ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	spartan-3e-	Oleg	Odintso	978	4			50			0.33	4.0	4.2	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
A		ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	spartan-6-3	James	Brakef	807	6			80	##	14.7	0.33	4.0	8.2	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
A	1	ag_6502	ag_6502 soft cor	beta	Oleg Odintsov	6502	8	8x	kintex-7-3	James	Brakef	824	6			176	##	14.7	0.33	4.0	17.7	verilog	2	ag_6502		yes	N	N	64K	64K	Y				2012	2012	6502 data sheets	verilog code generation, "phase level accurate"	
B		agcnorm	Apollo Guidance	beta	Dave Roberts	?	16	16											1.0		vhdl	5	AGC	some		N		32M	32M					2010	2012		Apollo Guidance Computer via NOR gate emulation	
X		altium/TSK165x		proprietar	Altium	PIC16	8	12	cyclone-2	Altium		428	4			50			0.33	1.0	38.6	not avail			yes	yes	N	Y	256	4K	Y				2004		CR0140.pdf, CR0114.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
X	1	altium/TSK165x		proprietar	Altium	PIC16	8	12	spartan-3-5	Altium		416	4			50			0.33	1.0	39.7	not avail			yes	yes	N	Y	256	4K	Y				2004		CR0140.pdf, CR0114.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
W		altium/TSK3000A		proprietar	Altium	RISC	32	32	cyclone-2	Altium		2664	4		6	50			1.00	1.0	18.8	not avail			yes	yes	N	N	4G	4G	Y				2004		CR0140.pdf, http://te	asm, C, C++, schem, VHDL & Verilog	default clock: 50MHz, opt mult/div
W	1	altium/TSK3000A		proprietar	Altium	RISC	32	32	spartan-3-5	Altium		2426	4		4	50			1.00	1.0	20.6	not avail			yes	yes	N	N	4G	4G	Y				2004		CR0140.pdf, http://te	asm, C, C++, schem, VHDL & Verilog	default clock: 50MHz, opt mult/div
X		altium/TSK51A		proprietar	Altium	8051	8	8x	cyclone-2	Altium		2135	4		1	50			0.33	6.0	1.3	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.PDF, CR0115.	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
X	1	altium/TSK51A		proprietar	Altium	8051	8	8x	spartan-3-5	Altium		1890	4		1	50			0.33	6.0	1.5	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.PDF, CR0115.	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
X		altium/TSK80x		proprietar	Altium	Z80	8	8x	cyclone-2	Altium		2568	4			50			0.33	3.0	2.1	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.pdf, CR0117.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
X	1	altium/TSK80x		proprietar	Altium	Z80	8	8x	spartan-3-5	Altium		2558	4			50			0.33	3.0	2.2	not avail			yes	yes	N	N	64K	64K	Y				2004		CR0140.pdf, CR0117.p	asm, C, C++, schem, VHDL & Verilog	default clock speed is 50MHz
W		altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	cyclone-2	James	Brakef	3144	4			87	##	q11.1	1.00	2.0	13.8	system v	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipeline	LPMs & systemVerilog
W		altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	cyclone-4-6	James	Brakef	3002	4			88	##	q13.1	1.00	2.0	14.6	system v	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipeline	LPMs & systemVerilog
W		altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	arria-2	James	Brakef	1815	A			163	##	q13.1	1.00	2.0	44.9	system v	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipeline	LPMs & systemVerilog
W		altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	spartan-3e-	James	Brakef	2689	4			75	##	i14.7	1.00	2.0	14.0	system v	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipeline	xilinx S3 primitives
W		altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	spartan-6-3	James	Brakef	1837	6			115	##	i14.7	1.00	2.0	31.4	system v	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipeline	xilinx S3 primitives
W	1	altor32_lite	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James	Brakef	1928	6			236	##	i14.7	1.00	2.0	61.3	system v	7	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000, no pipeline	xilinx S3 primitives
W		altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	cyclone-2	James	Brakef	3952	4		33	67	##	q11.1	1.00	1.0	16.9	system v	17	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
W		altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	cyclone-4-6	James	Brakef	3874	4		17	81	##	q13.1	1.00	1.0	21.0	system v	17	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
W		altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	arria-2	James	Brakef	2346	A		6	141	##	q13.1	1.00	1.0	60.1	system v	17	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	LPMs & systemVerilog
W		altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	spartan-3e-	James	declar	3897	4		9	61	##	i14.7	1.00	1.0	15.6	system v	16	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	xilinx S3 primitives
W		altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	spartan-6-3	James	Brakef	2546	6		9	91	##	i14.7	1.00	1.0	35.9	system v	16	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	xilinx S3 primitives
W	1	altor32	AltOr32	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James	Brakef	2602	6		5	176	##	i14.7	1.00	1.0	67.5	system v	16	altor32	yes	yes	N	Y	4G	4G	Y				2012	2014	OpenRISC 1000	simplified OpenRISC 1000	xilinx S3 primitives
W	1	alwcpu	Alwcpu	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James	Brakef	298	6			237	##	14.7	0.67	1.0	533.3	vhdl	7	top	some		N		64K	64K	Y		16		2009	2009		lightweight CPU	
A		amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	spartan-6-3	James	Brakef	6901	6		4	40	##	14.7	0.75	1.0	4.3	verilog	25	a23_core	yes	yes	N		4G	4G	Y			3	2010	2013	ARM7 data sheets	no MMU, shared cache	2048 LUTs used as single port RAM
A	1	amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James	Brakef	6409	6		2	82	##	14.7	0.75	1.0	9.6	verilog	25	a23_core	yes	yes	N		4G	4G	Y			3	2010	2013	ARM7 data sheets	no MMU, shared cache	2048 LUTs used as single port RAM
A		amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	spartan-6-3	James	Brakef	12834	6		8	40	##	14.7	1.05	1.0	3.3	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	4096 LUTs used as single port RAM
A		amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James	Brakef	12450	6		4	98	##	14.7	1.05	1.0	8.2	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	4096 LUTs used as single port RAM
A	1	amber	*Amber ARM-con*	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James	Brakef	7926	6		320	92	##	v14.1	1.05	1.0	12.2	verilog	25	a25_core	yes	yes	N	Y	4G	4G	Y			5	2010	2013	ARM7 data sheets	no MMU, data & inst caches	2454 LUTs used as single port RAM
A		ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	Aleksander O		91256	4	22	106	39		q13.1	1.00	1.0	0.4	verilog	85	soc	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	running on Terasic DE2-115 board
A	1	ao486	ao486	beta	Aleksander Osman	x86	32	8x	cyclone-4-7	James	Brakef	36094	4	4	47	46	##	q13.1	1.00	1.0	1.3	verilog	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
A		ao486	ao486	beta	Aleksander Osman	x86	32	8x	arria-2	James	syntax errors	A					##	q13.1	1.00	1.0		system v	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
A		ao486	ao486	beta	Aleksander Osman	x86	32	8x	kintex-7-3	James	syntax errors	6					##	14.7	1.00	1.0		system v	85	ao486	yes	yes			4G	4G	Y				2014	2014	x86 data sheets	complete 486, SoC configuration	non-SoC, no MMU
A	1	ao68000	ao68000	beta	Aleksander Osman	68000	16	16x	arria-2	James	Brakef	3479	A		6	169	##	q13.1	0.67	3.0	10.8	verilog	1	ao68000	some	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses microcode, instruction prefetch buffer	
B		aoocs	aoOCS - Wishbo	beta	Aleksander Osman	68000	16	16x	cyclone-3	James	pin constraint	4						q13.1	0.67	4.0		verilog	22	aoOCS	some	yes	N		4G	4G	Y				2010	2011	68000 data sheets	uses ao68000 core, Amiga chip set emulation (blitter, copper), Minimig alternative	
A		aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	cyclone-2	James	Brakef	5237	4	2	32	33	##	q11.1	1.00	1.0	6.3	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
A		aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	cyclone-4-6	James	Brakef	6034	4		32	43	##	q13.1	1.00	1.0	7.2	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
A		aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	arria-2	James	Brakef	3209	A	4	32	70	##	q13.1	1.00	1.0	22.0	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
A		aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	spartan-3-5	James	Brakef	5618	4	2	32	31	##	14.7	1.00	1.0	5.5	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
A		aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	spartan-6-3	James	Brakef	4180	6	2	12	49	##	14.7	1.00	1.0	11.8	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
A	1	aquarius	aquarius	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James	Brakef	4071	6	2	10	97	##	14.7	1.00	1.0	23.7	verilog	21	top	yes	yes	N		4G	4G	Y				2003	2009	SuperH data sheets		
		ARC		proprietar	Synopsys		32	16												1.0		not avail							4G	4G							range of reduced SPARC? uP	

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
A	1	ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	arria V	altera		4500	A			1050			2.50	1.0	583.3	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
A		ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	cyclone V	altera		4500	A			925			2.50	1.0	513.9	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	altera data sheets	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
A		ARM_Cortex_A9		ASIC	ARM	ARM a9	32	16	zynq	xilinx		4500	6			1000			2.50	1.0	555.6	asic			yes	yes	Y		4G	4G	Y	80	16	10		2012	xilinx plan ahead: an /	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
A		arm4u	ARM4U	stable	Joanathan Masur, Xavi	ARM7	32	32	cyclone-2	James Brakef		2084	4	3	12	43	##	q11.1s	0.75	1.0	15.4	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory
A		arm4u	ARM4U	stable	Joanathan Masur, Xavi	ARM7	32	32	cyclone-4-6	James Brakef		2809	4		8	43	##	q13.1	0.75	1.0	11.5	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory
A	1	arm4u	ARM4U	stable	Joanathan Masur, Xavi	ARM7	32	32	aria-2	James Brakef		1668	A	4	8	66	##	q13.1	0.75	1.0	29.5	vhdl	12	cpu	yes	ues	N		4G	4G	Y	80	16	5	2013	2014	ARM7 data sheets	university project	altera memory
		aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	arria-2	James	xilinx primitiv		A				##	q13.1	1.00	1.0		verilog	10	DLX_top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
A	1	aspida	ASPIDA DLX core	stable	Sotiriou	DLX	32	32	kintex-7-3	James Brakef		3586	6			257	##	14.7	1.00	1.0	71.7	verilog	10	DLX_top	yes	yes			4G	4G					2002	2009	Knuth DLX		compiled sync version
W		atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakef		810	A	2	0	123	##	q13.1	0.80	1.0	121.2	vhdl	8	ATLAS_CF	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
W		atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-6	James Brakef		643	6	1	0	103	##	14.7	0.80	1.0	127.9	vhdl	8	ATLAS_CF	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
W		atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef		648	6	1	0	168	##	14.7	0.80	1.0	207.6	vhdl	8	ATLAS_CF	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
W	1	atlas_core	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef		559	6	1	0	200	##	v14.1	0.80	1.0	286.2	vhdl	8	ATLAS_CF	yes	asm	N	Y	64K	64K	Y	80	8		2013	2014	opencore page	ARM thumb like inst set	non-MMU version
W		atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-3a-	Stephan Nolt		2406	4	1	11	81	##	14.7	0.80	1.0	27.0	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
W		atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	cyclone-4-6	Stephan Nolt		2967	4	1	32	99	##	q13.1	0.80	1.0	26.7	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
W		atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	cyclone-2	James Brakef		2711	4	1	74	71	##	q11.1s	0.80	1.0	21.0	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
W		atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	arria-2	James Brakef		1624	A	2	32	118	##	q13.1	0.80	1.0	58.3	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
W		atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-3a-	James Brakef		2450	4	1	9	76	##	14.7	0.80	1.0	24.9	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
W		atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	spartan-6-3	James Brakef		1545	6	1	10	100	##	14.7	0.80	1.0	51.5	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
W	1	atlas_2K	Atlas Processor (	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James Brakef		1512	6	1	5	149	##	14.7	0.80	1.0	79.1	vhdl	19	ATLAS_2K	yes	asm	N	Y	64K	64K	M	80	8		2013	2014	opencore page	ARM thumb like inst set	has MMU & full SOC features
A	1	avr_core	avr_core	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James Brakef		2135	6			127	##	14.7	0.33	1.0	19.7	verilog	15	avr_core	yes	yes	N		64K	128K	Y		32		2002	2012	AVR data sheets	VHDL core included	
A		avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	1 slot	1199	6			127	##	14.7	0.33	1.0	35.0	vhdl	9	avr_core	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
A	1	avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	2 slot	1554	6			223	##	14.7	0.33	1.0	47.4	vhdl	10	avr_core_	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
A		avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	3 slot	1812	6			243	##	14.7	0.33	1.0	44.2	vhdl	10	avr_core_	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
A		avr_hp	avr_hp	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	4 slot	2054	6			278	##	14.7	0.33	1.0	44.7	vhdl	10	avr_core_	some	yes	N		64K	128K	Y		32		2010	2010	AVR data sheets	hyper pipelined (eg barrel) AVR	
A	1	avr8	Reduced AVR Co	beta	Nick Kovach	AVR	8	16	kintex-7-3	James Brakef		174	6			418	##	14.7	0.33	1.0	792.2	verilog	1	rAVR	yes	yes	N		64K	64K	Y	17	4		2010	2010	AVR data sheets	not a full clone, doc is opencores page	
A	1	avrtinyx61cor	avrtinyx61core	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James Brakef		1243	6			194	##	14.7	0.33	1.0	51.5	vhdl	1	mcu_core		yes	N		64K	128K	Y		32		2008	2009	AVR data sheets		
A		ax8	AX8 MCU	stable	Daniel Wallner	AVR	8	16	spartan-6-3	James	missing ROM		6					14.7	0.33	1.0		vhdl	14	A90S1200			N		64K	128K	Y		32		2002	2009	AVR data sheets	both A90S1200 & A90S2313	80K LUTs as ROM
		b16		stable	Bernd Paysan	forth	16	5	arria-2	James Brakefield			A					q13.1	0.67	1.0		verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16	two versions: one/15 source files, derived from c18	
		b16		stable	Bernd Paysan	forth	16	5	spartan-3-5	James Brakefield			4					14.7	0.67	1.0		verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16	two versions: one/15 source files, derived from c18	
W	1	b16		stable	Bernd Paysan	forth	16	5	spartan-6-3	James Brakef		554	6			134	##	14.7	0.67	1.0	161.7	verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16	two versions: one/15 source files, derived from c18	
		b16		stable	Bernd Paysan	forth	16	5	kintex-7-3	James Brakef	source	6					##	14.7	0.67	1.0		verilog	1	b16	yes	yes	N								2002	2011	bernd-paysan.de/b16	two versions: one/15 source files, derived from c18	
W	1	ba22		proprietar	CAST Inc	RISC	32	16x	spartan-6	CAST Inc		1800	6		32	72			1.00	1.0	40.0	not avail							4G	4G			32				www.cast-inc.com		
W	1	blue	16-bit CPU Blue	stable	Al Williams	accum	16	16	spartan-3-5	James	remov	1025	4			63	##	14.7	0.67	1.0	41.1	verilog	16	topbox	web		N		4K	4K	N	16	2		2009	2010		Caxton Foster's Blue derivative	http://www.youtube.com/watch?v=dt4zezZP8v
X	1	bobcat		beta	Stan Drey		16	24	kintex-7-3	James Brakef		1622	6	1		107	##	14.7	0.67	1.0	44.0	vhdl							64K	64K					1998			appears to be a DSP	
		c0or1k	Codezero OpenR	planning	Drasko Draskovic	RISC																no code												2010			C code for simulation	
W	1	c16	16 Bit Microcont	stable	Jsauermann	C	16	8x	spartan-3-5	James Brakef		1751	4		16	57	##	14.7	0.33	1.0	10.7	vhdl	22	Board_cp	min	C,asm	N		64K	64K	Y		5		2003	2012		8080 derivative, optional UART, 8-bit r	xilinx 4K RAM primitives
		cf_ssp	CF State Space P	stable	Tom Hawkins	?																confluence												2003	2009		confluence to VHDL	
X	1	cole_c16		beta	Cole Design & Develop	RISC	16	16	spartan-6-3	James Brakef		554	6			298	##	14.7	0.67	7.0	51.4	vhdl	1	core	yes	asm	N		64K	64K	N	20	8		2002	2012		(7) clks per inst, complete SOC	for teaching
A		copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	cyclone-2	James	missin	1348	4			77	##	q11.1s	0.33	2.0	9.5	vhdl	16	cp_copyb	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	
A		copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	cyclone-4-6	James	missin	1345	4			104	##	q13.1	0.33	2.0	12.7	vhdl	16	cp_copyb	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	
A		copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	arria-2	James	missin	604	A			167	##	q13.1	0.33	2.0	45.6	vhdl	16	cp_copyb	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	
A		copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	spartan-3e-	James	missin	875	4			79	##	14.7	0.33	2.0	14.9	vhdl	16	cp_copyb	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	
A		copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	spartan-6-3	James	missin	619	6			86	##	14.7	0.33	2.0	22.8	vhdl	16	cp_copyb	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	
A	1	copyblaze	copyBlaze	stable	Abdallah Ellbrahimi	picoBlaze	8	18	kintex-7-3	James	missin	622	6			217	##	14.7	0.33	2.0	57.5	vhdl	16	cp_copyb	yes	asm	N		256	2K	Y				2011	2013	microBlaze data shee	wishbone extras	
		cortex_m3	cortex_m3	?	Strauch Tobias	ARM c3	32	16														no files												2013		cortex M3 data sheet	claims to be mature	
		cowgirl	Cowgirl	beta	Thebeekeeper		16	16	kintex-7-3	James	empty design		6					14.7	0.67	1.0		vhdl	14	cowgirl						64K				2006	2009			
X	1	cpu16		beta	C. H. Ting	forth	16	5	kintex-7-3	James	case c	367	6			355	##	14.7	0.67	1.0	648.1	vhdl	1	cpu16	yes	asm	N		64K	64K		28			2000			part of eForth?	data width can be expanded
A	1	cpu6502_true	cpu6502_tc	stable	Jens Gutschmidt	6502	8	8x	kintex-7-3	James Brakef		1678	6			159	##	14.7	0.33	4.0	7.8	vhdl	7	r6502_tc		yes	N	N	64K	64K	Y				2008	2010	6502 data sheets		
A		cpu65c02_tru	cpu65c02_tc	stable	Jens Gutschmidt	6502	8	8x	spartan-6-3	James	latch v	4794	6			47	##	14.7	0.33	4.0	0.8	vhdl	8	core		yes	N	N	64K	64K	Y				2008	2013	6502 data sheets		
A	1	cpu8080	8080 Compativle	stable	Scott Moore	8080	8	8x	spartan-6-3	James Brakef		1269	6			129	##	14.7	0.33	9.0	3.7	verilog	1	m8080	yes	yes	N	N	64K	64K	Y				2006	2009	8080 data sheets	includes VGA display generator, three variants	
A	1	cpu86		beta	ht-lab.com	8086	8	8x	kintex-7-3	James Brakef		3421	6	1		127	##	14.7	0.17	2.0	3.1	vhdl	23	cpu86_to	yes	yes	N	N	1M	1M	Y				2002	2010	x86 data sheets	8088 clone	www.ht-lab.com
		cpugen	Cpu Generator	stable	Giovanni Ferrante																													2003	2009		x86 executable that generates VHDL uP	
B		cqpic		stable	Sumio Morioka	PIC16	8	14	arria-2	James	ROM paramet		A				##	q13.1	0.67	1.0		vhdl & v	5	CQPIC	yes	yes	N	Y	256	4K	Y				1999	2004	PIC16 data sheets	LPM macros	http://www002.upp.so-net.ne.jp/morioka/cqpi
A	1	cray1		alpha	Christopher Fenton	cray1	64	16	kintex-7-3	James Brakef		13463	6	19	10	127	##	14.7	6.00	1.0	56.6	verilog	46	cray_sys_	yes	yes	Y	N	4M	4M	N		512		2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew-cray-1a/
A		cray1		alpha	Christopher Fenton	cray1	64	16	kintex-7-3	James	missing black		6				##	v14.1	6.00	1.0		verilog	46	cray_sys_	yes	yes	Y	N	4M	4M	N		512		2010		CRAY data sheets	homebrew Cray1	www.chrisfenton.com/homebrew-cray-1a/
		crisc_cpu	CRISC CPU	planning	Andre Adrian	68000 like	16	16x														no files					N		4G	4G	Y	20	15		2011			see opencores web page: both 16-bit & 32-bit registers, 11 addressing modes	
A	1	dalton_8051		stable	Tony Givargis	8051	8	8x	kintex-7-3	James Brakef		2725	6	1	1	105	##	14.7	0.33	1.0	12.7	vhdl	7	i8051_all	yes	yes	N	N	64K	64K	Y				1999	2003	8051 data sheets	ASIC	www.cs.ucr.edu/~dalton/
X		dataflow_chapman		alpha	Rob Chapman, Steven	forth			kintex-7-3	James	file WebCase		6					14.7	0.33	1.0		vhdl	27	DataFlow	yes		N		256	256					2003			course work	
W	1	dcpu16		beta	Marcus Persson , Shaw	RISC	16	16	kintex-7-3	James Brakef		662	6	1		318	##	14.7	0.67	4.0	80.4	vhdl & v	5	dcpu16_c	yes	asm	N	N	64K	64K	N	37	8		2009	2012	https://github.com/d	for the 0X10c game	4+ addressing modes, 4 & 5-bit reg /modefields
A	1	df6805		proprietar	Hitech Global	6805	8	8x	stratix-1	Hitech Globa		1690	4			83			0.33	4.0	4.1	not avail			yes	yes	N	N	64K	64K	Y						6805 data sheets		www.hitechglobal.com/IPCores/DF6805.htm
W		dfp	dfp	stable	Ron Chapman	forth	8	Y	spartan-6-3	James Brakef		334	6			112	##	14.7	0.33	1.0	110.7	vhdl	25	DataFlow	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
W	1	dfp	dfp	stable	Ron Chapman	forth	8	Y	kintex-7-3	James Brakef		297	6			192	##	14.7	0.33	1.0	213.2	vhdl	25	DataFlow	yes										2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
X	1	diogenes	diogenes	beta	Fekknhifer	RISC	16	16	kintex-7-3	James Brakef		807	6		1	297	##	14.7	0.67	1.0	246.3	vhdl	11	cpu	yes	yes	N			1K					2008	2009		"student RISC system"	
		distributed_ir	Distributed limit	planning	Leo Ger		16	16														vhdl	11	mini_uP_x16			N		64K	64K					2009	2009		single stack and 4 data registers	
W	1	dragonfly		beta	LEOX team	MISC	16	16	kintex-7-3	James Brakef		788	6			164	##	14.7	0.67	1.0	139.3	vhdl	6	dgf_core	yes		N		256	2K					2001		www.leox.org	unusual, uses FIFOs	
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	cyclone-4-6	James Brakef		5153	4			79	##	q13.1	1.00	1.5	10.2	verilog	23	eco32	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakef		4564	4		10	51	##	14.7	1.00	1.5	7.4	verilog	23	eco32	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	downloaded ISE project run, has *.ucf
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	cyclone-2	James Brakef		4840	4		2	56	##	q11.1s	1.00	1.5	7.8	verilog	17	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	cyclone-4-6	James Brakef		5153	4			79	##	q13.1	1.00	1.5	10.2	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	arria-2	James Brakef		2711	A			116	##	q13.1	1.00	1.5	28.6	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-3-5	James Brakef		3034	4		2	55	##	14.7	1.00	1.5	12.0	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	spartan-6-3	James Brakef		2271	6		1	92	##	14.7	1.00	1.5	27.0	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
X		eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	atrix-7-3	James Brakef		2107	6		1	121	##	14.7	1.00	1.5	38.4	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
X	1	eco32	SOC:ECO32	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakef		2210	6		1	160	##	14.7	1.00	1.5	48.1	verilog	23	cpu	yes	yes	N		512M	256M	Y	61	32		2003	2014		MIPS like, slow mul & div	
		ecpu	ecpu	planning	Sahrfili Matturi																	verilog												2009	2009			
X		edge	Edge Processor (	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	Hesha	unkown modu		6	7		50		14.7	1.00	1.0		verilog	30	edge_atly	yes	yes	N	N	4G	4G	Y		32	5	2014		MIPS data sheets	MIPS1 clone, on Atlys Spartan-6 LX45	
X	1	edge	Edge Processor (	alpha	Hesham ALMatary	MIPS	32	32	spartan-6-3	James Brakef		5345	6	7	1	8	##	14.7	1.00	1.0	1.5	verilog	30	edge_cor	yes	yes	N	N	4G	4G	Y		32	5	2014		MIPS data sheets	MIPS1 clone	
		edu_3bus_ar	Educational 3 Bu	spec	Ayman Mohamed	RISC	32	32														no files									33	32		2012	2013			
X		eight_bit_uc		stable	Synplicity	RISC	8	12	kintex-7-3	James	signal/variable		6					14.7	0.67	1.0		vhdl	10	eight_bit_uc						2K	Y		32				part of Amplify documentation	
		elm	ELM Embedded	alpha	David Sheffield, Curt Harting																	no files												2010	2010			
		encore	Encore	planning	Aloy Ambergen																	no files												2010	2011			
W		ensilica		proprietar	ensilica.com	eSi-1600	16		virtex-5	ensilica		1100	6			160			0.67	1.0	97.5	not avail			yes	yes	N		64K	64K			16			www.ensilica.com	verilog source included with license	10 addressing modes
W	1	ensilica		proprietar	ensilica.com	eSi-3200	32		stratix-4	ensilica		1800	A			200			1.00	1.0	111.1	not avail			yes	yes			4G	4G			16	5		www.ensilica.com	verilog source included with license	10 addressing modes
		eric5		proprietar	entner-electronics.com	forth	9	9	cyclone-4-6	enter-electronics.com			4	opt		60			0.67	1.0		not avail							512	128K			3-4		2007		40 MIPS: ERIC5+, ERIC5Q+	
W	1	eric5		proprietar	entner-electronics.com	forth	9	8	cyclone-4-6	enter-electro		110	4	opt		60			0.42	1.0	229.1	not avail							512	1K			3-4		2007		25 MIPS: ERIC5xs, ERIC5Q	
X	1	erp	Educational RISC	stable	Shahzadjk	RISC	8	16	spartan-3-5	James Brakef		366	4	1	1	70	##	14.7	0.33	1.0	63.5	verilog	1	ERPverilo	yes							15	6		2004	2009		two report PDFs & one Verilog file	
X		erp	Educational RISC	stable	Shahzadjk	RISC	8	16	kintex-7-3	James	4K primitives		6				##	14.7	0.33	1.0		verilog	1	ERPverilo	yes							15	6		2004	2009		two report PDFs & one Verilog file	
A	1	fpgammix		stable	Tommy Thorn	MMIX	64	32	arria-2	James Brakef		11605	A	8	10	94	##	q13.1	1.50	4.0	3.0	system v	2	core	yes	yes	Y	Y	4G	4G	Y	256	288		2006	2008		clone of Knuth's MMIX	micro-coded
		fpgammix		stable	Tommy Thorn	MMIX	64	32	kintex-7-3	James	unacceptable		6				##	14.7	1.50	4.0		system v	2	core	yes	yes	Y	Y	4G	4G	Y	256	288		2006	2008		clone of Knuth's MMIX	micro-coded
A	1	free_risc8		stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakef		355	6			142	##	14.7	0.33	1.0	132.2	verilog	8	cpu	yes	yes	N			256	4K	Y				2002	2011	PIC16 data sheets		
A		free6502		stable	David Kessner	6502	8	8x	spartan-6-3	James Brakef		663	6			89	##	14.7	0.33	4.0	11.1	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
A	1	free6502		stable	David Kessner	6502	8	8x	kintex-7-3	James Brakef		646	6			193	##	14.7	0.33	4.0	24.6	vhdl	5	free6502	yes	yes	N	N	64K	64K	Y				1999	2000	6502 data sheets	microcoded	
A		gl85		stable	Alex Miczo	8085	8	8x	kintex-7-3	James	gate level des		6					14.7	0.33	4.0		vhdl	1	i8085	yes	yes	N	N	64K	64K	Y				1993		8085 data sheets	also a TTL implementation in VHDL	
		gullwing		simulatior	Charles LaForest	forth	32	5														no code			yes	asm	N		4K	4K					2007		BS thesis	virtual stack machines vs RISC	MuP21 clone
W		gumnut		stable	Peter Ashenden	RISC	8	18	cyclone-2	James Brakef		3110	4		18	53	##	q11.1s	0.33	1.0	5.7	verilog	6	gumnut_v	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
W		gumnut		stable	Peter Ashenden	RISC	8	18	cyclone-4-6	James Brakef		3102	4		9	68	##	q13.1	0.33	1.0	7.2	verilog	6	gumnut_v	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
W		gumnut		stable	Peter Ashenden	RISC	8	18	arria-2	James Brakef		1264	A		9	120	##	q13.1	0.33	1.0	31.2	verilog	6	gumnut_v	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
W		gumnut		stable	Peter Ashenden	RISC	8	18	spartan-3-5	James Brakef		415	4		6	74	##	14.7	0.33	1.0	59.1	verilog	6	gumnut_v	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
W		gumnut		stable	Peter Ashenden	RISC	8	18	spartan-6-3	James Brakef		306	6		5	118	##	14.7	0.33	1.0	126.9	verilog	6	gumnut_v	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
W		gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakef		305	6		3	185	##	14.7	0.33	1.0	200.4	verilog	6	gumnut_v	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
W		gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakef		335	6		3	178	##	14.7	0.33	1.0	175.8	vhdl	20	gumnut_v	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
W	1	gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakef		388	6			259	##	14.7	0.33	1.0	220.7	verilog	6	gumnut-r	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
W		gumnut		stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakef		420	6			275	##	14.7	0.33	1.0	216.2	vhdl	9	gumnut-r	yes	asm	N	Y	256	4K	Y		8		2007		http://digitaldesign.as	see Digital Design: An Embedded Systems Approach Using VHDL	
A		gup	HC11 Compatibl	stable	Kevin Phillipson	68HC11	8	8x	arria-2	James Brakef		925	A	1	1	127	##	q13.1	0.33	4.0	11.3	vhdl	25	gator_up	yes	yes	N	N	64K	64K	Y				2008	2009	6811 data sheets	68HC11 compatible	top level is schematic
A		hc11core		stable	Green Mountain Comp	68HC11	8	8x	arria-2	James Brakef		1962	A			116	##	q13.1	0.33	4.0	4.9	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with corrections	http://www.gmvhdl.com/hc11core.html
A	1	hc11core		stable	Green Mountain Comp	68HC11	8	8x	kintex-7-3	James Brakef		2190	6			127	##	14.7	0.33	4.0	4.8	vhdl	1	hc11rtl	yes	yes	?	N	64K	64K	N	53	8	2	2000		6811 data sheets	restricted use license, with corrections	http://www.gmvhdl.com/hc11core.html
A		hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-3-5	James Brakef		1937	4	1	3	20	##	14.7	0.33	4.0	0.9	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
A	1	hd63701	HD63701 compa	planning	Tsuyoshi Hasegawa	6801	8	8x	spartan-6-3	James Brakef		1412	6	1	3	31	##	14.7	0.33	4.0	1.8	verilog	6	HD63701_CORE			N	N	64K	64K	Y				2014			Used in Atari game console, 6801 clone?	
X		hicovec	HiCoVec a config	beta	Harald Manske, Gundo	RISC	32	32	kintex-7-3	James	compiler erro		6					14.7	1.00	1.0		vhdl	28	cpu	yes	asm	N				Y				2008	2010		hybrid scalar & vector processor	
W		hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-3	Eric Wallin		1800	4	4	3	200		q13.0	1.00	1.0	111.1	verilog			yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
W		hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-2	James Brakef		1633	4	4	44	169	##	q11.1s	1.00	1.0	103.4	verilog		core	yes		N				N	40	10	8	2013	2014		4 symetrical stacks, eight threads via pipeline barrel	
W		hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-4	James Brakef		3046	4		14	115	##	q13.1	1.00	1.0	37.6	verilog		core	yes		N				N	40	10	8	2013	2014		4 symetrical stacks, eight threads via pipeline barrel	
W		hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	James Brakef		1256	A	6	3	217	##	q13.1	1.00	1.0	172.5	verilog		core	yes		N				N	40	10	8	2013	2014		4 symetrical stacks, eight threads via pipeline barrel	
W	1	hive	hive	stable	Eric Wallin	4-8 stack	32	16	arria-2	James Brakef		905	A	8	20	284	##	q13.1	1.00	1.0	313.4	verilog		core	yes		N				N	40	10	8	2013	2014		4 symetrical stacks, eight threads via pipeline barrel	
W		hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-2	James Brakef		2375	4	4	52	165	##	q11.1s	1.00	1.0	69.6	verilog		hive_core	yes		N				N	40	10	8	2013	2014		8 symetrical stacks, eight threads via pipeline barrel	
W		hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-4	James Brakef		3792	4		29	115	##	q13.1	1.00	1.0	30.5	verilog		hive_core	yes		N				N	40	10	8	2013	2014		8 symetrical stacks, eight threads via pipeline barrel	
W		hive	hive	stable	Eric Wallin	4-8 stack	32	16	cyclone-5	James Brakef		1290	A	6	24	177	##	q13.1	1.00	1.0	137.1	verilog		hive_core	yes		N				N	40	10	8	2013	2014		8 symetrical stacks, eight threads via pipeline barrel	
W		hive	hive	stable	Eric Wallin	4-8 stack	32	16	arria-2	James Brakef		1387	A	8	24	283	##	q13.1	1.00	1.0	204.4	verilog		hive_core	yes		N				N	40	10	8	2013	2014		8 symetrical stacks, eight threads via pipeline barrel	
		hive	hive	stable	Eric Wallin	4-8 stack	32	16	spartan-6-3	James	missing port n		6				##	14.7	1.00	1.0		verilog		core	yes		N				N	40	10	8	2013	2014		4-8 symetrical stacks, eight threads via pipeline barrel	
		hivek		alpha	Hadley Magno	VLIW	32													1.0		vhdl	18	hivek										2013			two inst per clock	incomplete source code
		hmta	HyperMTA	planning	Mahesh Palve	accum	8	16														no files					Y					64		2002	2009		up to 256 threads	
X	1	hpc-16	HPC-16	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakef		875	6			136	##	14.7	0.67	1.0	104.2	vhdl	20	cpu	yes	asm	N		64K	64K			16		2005	2009			
		ic6821	vhdl core of IC68	beta	Ttsenis		8													1.0		vhdl	1	VHDL682	yes									2005	2009	6800 data sheets	VHDL for M6821	
X	1	iDEA		alpha	Hui Yan Cheah etal	RISC	16	32	virtex-6	Liu Cheah		321	6	1	2	405		13.2	0.67	1.0	845.3	verilog	22	cpu_top	yes	yes	N	Y	64K	64K	N	24	32	9	2011	2014	The iDEA DSP Block B	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual results
X		iDEA		alpha	Hui Yan Cheah etal	RISC	16	32	artic-7	Liu Cheah		324	6	1	2	281		13.2	0.67	1.0	581.1	verilog	22	cpu_top	yes	yes	N	Y	64K	64K	N	24	32	9	2011	2014	The iDEA DSP Block B	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual results
X		iDEA		alpha	Hui Yan Cheah etal	RISC	16	32	kintex-7	Liu Cheah		343	6	1	2	410		13.2	0.67	1.0	800.9	verilog	22	cpu_top	yes	yes	N	Y	64K	64K	N	24	32	9	2011	2014	The iDEA DSP Block B	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual results
X		iDEA		alpha	Hui Yan Cheah etal	RISC	16	32	virtex-7	Liu Cheah		324	6	1	2	378		13.2	0.67	1.0	781.7	verilog	22	cpu_top	yes	yes	N	Y	64K	64K	N	24	32	9	2011	2014	The iDEA DSP Block B	uses DSP slice in barrel mode for ALU	GitHub version is simulation only
		ignite_ptsc		proprietar	George Shaw	forth	32	8												1.0		not avail					N		4G	4G					1995	2002		ShBoom clone, fast ASIC with high coding density	
		inst_list_proc	8-bit Pipelined P	planning					kintex-7-3	James Brakefield			6				##	14.7	0.33	1.0		verilog	34	top	yes		N								2014				
A		ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	cyclone-2	Jose Ruiz		2349	4			50		q11.1	1.00	1.0	21.3	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki	MIPS R3000 clone	originally MIPS-I moving to MIPS32r1
A		ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	spartan-3	Jose Ruiz		3173	4			51		14.3	1.00	1.0	16.1	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki	MIPS R3000 clone	originally MIPS-I moving to MIPS32r1
A		ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	virtex-5	Jose Ruiz		2017	6			104		14.3	1.00	1.0	51.6	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki	MIPS R3000 clone	originally MIPS-I moving to MIPS32r1
A	1	ion	Ion MIPS compa	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakef		1533	6			163	##	14.7	1.00	1.0	106.0	vhdl	12	mips_soc	yes	yes	N		4G	4G	Y		32		2011	2014	en.wikipedia.org/wiki	MIPS R3000 clone	originally MIPS-I moving to MIPS32r1
W	1	J1		stable	James Bowman	forth	16	16	spartan-6	James Brakef		333	6		1	117	##	14.7	0.80	1.0	280.2	vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
W		J1		stable	James Bowman	forth	16	16	kintex-7-3	James Brakef		387	6		4	133	##	14.7	0.80	1.0	274.6	verilog	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
		J1		stable	James Bowman	forth	16	16	kintex-7-3	James	syntax errors		6					14.7	0.80	1.0		vhdl	1	j1	yes	forth	N		64K	64K		16		2	2006	2010	excamera.com/sphinx	uCode inst, dual port block RAM	32 deep data & return stacks
X	1	jam		stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakef		1369	6			143	##	14.7	1.00	1.0	104.2	vhdl	17	cpu	yes		N	Y	128K	128K			32	5	2002			serial multiply & divide	
W	1	jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakef		723	6			178	##	14.7	0.33	1.0	81.4	vhdl	3	Processor	yes							27	16		2002			neural network microprocessor, specialized registers	

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hard	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
		jmr16f84	JMP16F84 PIC M	stable	Julio Rodriguez	PIC16	8	14											1.0		no files						Y							2013		PIC16 data sheets		
W	1	jop	JOP a Java Optim	stable	Martin Schoeberl etal	forth	16	16	cyclone-1	Martin	Schoe	2000	4			100		q10.0	0.67	1.0	33.5	vhdl	11	core	yes	yes	N		256K	256K				2004	2014	https://github.com/jo	leros is his later effort	java app builds some source code files
X		jpu16		stable	Joksan Alvarado	RISC	16	26	kintex-7-3	James	missing	RAM 1	6					14.7	0.67	1.0		vhdl	9	JPU16	yes	asm	N		64K	64K			16		2012	https://github.com/jo	32 deep call stack, 8 addressing modes	
A	1	k68	K68	alpha	Shawn Tan	68000	8	16x	kintex-7-3	James	Brakef	2392	6			24	##	14.7	0.67	4.0	1.7	verilog	15	k68_cpu	yes	yes	N	N	4K	4G	Y		16		2003	2009	68000 data sheets	68K binary compatible	
		klc32	KLC32	planning	Robert Finch	RISC	32	32														verilog	25	KLC32	yes		N		4G	4G	Y		32		2011	2012			
A	1	lattice6502	Lattice 6502	beta	Ian Chapman	6502	8	8x	kintex-7-3	James	Brakef	4942	6			214	##	14.7	0.33	4.0	3.6	vhdl	3	ghdl_proc	yes	yes	N	N	64K	64K	Y				2010	2010	6502 data sheets	targeted to LCMXO2280	huge LUT count
W	1	latticemicro32		stable	Yann Siommeau, Micha	RISC	32	32	arria_2	James	Brakef	2166	A	4	30	149	##	q13.1	0.80	1.0	55.0	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki	optional data & inst caches	
W		latticemicro32		stable	Yann Siommeau, Micha	RISC	32	32	spartan-6	James	Brakef	2093	6	3	15	85	##	14.7	0.80	1.0	32.4	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki	optional data & inst caches	
W		latticemicro32		stable	Yann Siommeau, Micha	RISC	32	32	kintex-7-3	James	Brakef	2292	6	3	8	155	##	14.7	0.80	1.0	54.2	verilog	24	lm32_cpu	yes	yes	N		4G	4G	Y		32		2006	2012	en.wikipedia.org/wiki	optional data & inst caches	
W	1	latticemicro8		stable	Lattice Semiconductor	RISC	8	18	LFE2	Lattice	Semic	265	4			104			0.33	2.0	64.4	vhdl	10	isp8_core	yes	yes	N		256	4K	Y		32		2005	2010	en.wikipedia.org/wiki	16 deep call stack, four configurations	
W		lem1_9	lem1_9	stable	James Brakefield	accum	1	9	cyclone-2	James	2 stag	237	4		1	138	##	q11.1	0.04	1.0	23.3	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	Block ROM inferred in 2 stage pipe version
W		lem1_9	lem1_9	stable	James Brakefield	accum	1	9	cyclone-4	James	2 stag	238	4		1	138	##	q13.1	0.04	1.0	23.1	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	Block ROM inferred in 2 stage pipe version
W		lem1_9	lem1_9	stable	James Brakefield	accum	1	9	arria-2	James	2 stag	167	A		1	299	##	q13.1	0.04	1.0	71.7	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	Block ROM inferred in 2 stage pipe version
W		lem1_9	lem1_9	stable	James Brakefield	accum	1	9	spartan-3-5	James	1 stag	85	4		1	157	##	14.5	0.04	1.0	73.7	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	
W		lem1_9	lem1_9	stable	James Brakefield	accum	1	9	spartan-6-3	James	1 stag	65	6		1	223	##	14.5	0.04	1.0	137.3	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	
W	1	lem1_9	lem1_9	stable	James Brakefield	accum	1	9	kintex-7	James	1 stag	63	6		1	358	##	14.5	0.04	1.0	227.2	vhdl	3	lem1_9m	yes	asm	N	Y	64	2K	N	8	64	1	2003	2009		logic emulation machine	
X	1	lemberg		stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4-6	James	Brakef	37459	4	25	54	43	##	q13.1	1.00	1.0	1.1	vhdl	57	core	yes	yes	Y		4G	2M	Y		32	4	2011		www2.imm.dtu.dk/~u	upto 4 inst/clock	LPM mem & floating point
X		lemberg		stable	Wolfgang Puffitsch	VLIW	32	32	arria-2	James	failed in fitter		A				##	q13.1	1.00	1.0		vhdl	57	core	yes	yes	Y		4G	2M	Y		32	4	2011		www2.imm.dtu.dk/~u	upto 4 inst/clock	LPM mem & floating point
A		leon		stable	Jiri Gaisler, Jan Anderss	SPARC	32	32				3500							1.0			vhdl	100s	leon3x	yes	yes	Y		4G	4G			64		2003	2013	SPARC data sheets	customized for ~50 FPGA boards, configurable	
W		leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	Martin	Schoe	189	4		1	160			0.67	1.0	567.2	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
W		leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3	Martin	Schoe	188	4		1	129			0.67	1.0	459.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
W	1	leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin	Schoe	112	6		1	182			0.67	1.0	1088.8	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
W		leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-2	James	Brakef	259	4		1	122	##	q11.1	0.67	1.0	316.5	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
W		leros	Leros	stable	Martin Schoeberl	accum	16	16	cyclone-4-6	James	Brakef	238	4		1	149	##	q13.1	0.67	1.0	420.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
W		leros	Leros	stable	Martin Schoeberl	accum	16	16	arria-2	James	Brakef	164	A		1	266	##	q13.1	0.67	1.0	1086.2	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
W		leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-3-5	James	Brakef	247	4		1	105	##	14.7	0.67	1.0	285.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
W		leros	Leros	stable	Martin Schoeberl	accum	16	16	spartan-6	James	Brakef	174	6		1	155	##	14.7	0.67	1.0	595.9	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
W		leros	Leros	stable	Martin Schoeberl	accum	16	16	kintex-7-3	James	Brakef	169	6		1	274	##	14.7	0.67	1.0	1084.7	vhdl	5	leros	yes	yes	N	Y	256	64K			2	2	2008	2012	Leros: A Tiny Microco	256 word data RAM, PIC like	short LUT inst ROM
		leros32	Leros-32	simulation	Jon Pry	accum	32	16	kintex-7-3	James	missing memory components											vhdl	10	leros_nexys2			N		4G	4G					2013		https://github.com/jo	see Leros entry, simulation only	missing several dual port RAMs
A		light52	Lightweight 8051	beta	Jose Ruiz	8051	8	8x	cyclone-2-7	Jose Ruiz		1339	4	1	29	62			0.33	6.0	2.5	vhdl	8	light52_c	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	0.0187 DMIPS/MHz, i8051 is 0.0094 DMIPS/MH
A		light52	Lightweight 8051	beta	Jose Ruiz	8051	8	8x	spartan-3-4	Jose Ruiz		1424	4	1	10	35			0.33	6.0	1.4	vhdl	8	light52_c	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to area	~ 6 clocks/inst
A	1	light52	Lightweight 8051	beta	Jose Ruiz	8051	8	8x	kintex-7-3	James	Brakef	1027	6	1	1	148	##	14.7	0.33	6.0	7.9	vhdl	8	light52_c	yes	yes	N	N	64K	64K	Y				2012	2013	8051 data sheets	targeted to balanced	~ 6 clocks/inst
A		light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-2-5	Jose Ruiz		203	4		4	60		q9.1	0.33	9.0	10.8	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to speed, bare core	typically 9 clocks per inst, .04=.33/9
A		light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	cyclone-2-7	Jose Ruiz		413	4		4	80		q9.0	0.33	9.0	7.1	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to balanced, bare core	typically 9 clocks per inst, .04=.33/9
A		light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-3-5	Jose Ruiz		209	4		1	100		q9.1	0.33	9.0	17.5	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to speed, bare core	typically 9 clocks per inst, .04=.33/9
A	1	light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James	Brakef	154	6		1	247		14.7	0.33	9.0	58.9	verilog	5	i80soc	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, includes UART, inter	typically 9 clocks per inst, .04=.33/9
A		light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James	Brakef	148	6		3	172	##	14.7	0.33	9.0	42.7	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/9
A		light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	kintex-7-3	James	Brakef	154	6		1	247	##	14.7	0.33	9.0	58.9	verilog	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/9
A		light8080	Lightweight 8080	stable	Jose Ruiz, Moti Litoche	8080	8	8x	spartan-6	James	Brakef	150	6		3	142	##	14.7	0.33	9.0	34.6	vhdl	5	light8080	yes	yes	N	N	64K	64K	Y				2007	2012	8080 data sheets	targeted to area, bare core	typically 9 clocks per inst, .04=.33/9
		lpu	LocationPU	planning	Bkorsedal																	no files												2002	2009		very early: minimal doc	
W	1	Lutiac		custom	David Galloway, David	reg	16	NA	stratix-4	David	Gallow	140	A	4		198			0.67	1.0	947.6	vhdl & verilog							64	N	64	32	3		2010	Lutiac – Small Soft Pro	synthesis maps PC into ucode	no inst mem: small state machine, ~200 inst op
		Lutiac		custom	David Galloway, David	reg	16	NA	stratix-4	David	Gallow	480	A	4		197			0.67	1.0	275.0	vhdl & verilog					Y		128	N	64	32	3		2010	Lutiac – Small Soft Pro	synthesis maps PC into ucode	no inst mem: large state machine, ~200 inst op
X	1	lwrisc	ClaiRISC	stable	Li Wu	accum	8	12	arria-2	James	Brakef	88	A		1	230	##	q13.1	0.17	1.0	443.6	verilog	9	risc_core		asm	N	Y	256	2K	Y	16			2008	2009		simplified PIC, 4 reg rtn stack	absolute addressing only, lowered MIPS/clk
A		m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	cyclone-2	James	Brakef	3752	4			70	##	q11.1	1.00	1.0	18.8	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
A		m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	cyclone-4	James	Brakef	3795	4			94	##	q13.1	1.00	1.0	24.8	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
A	1	m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	arria-2	James	Brakef	2101	A			190	##	q13.1	1.00	1.0	90.6	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
A		m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	spartan-3-5	James	Brakef	4688	4			70	##	14.7	1.00	1.0	14.9	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
A		m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	spartan-6-3	James	Brakef	3483	6			131	##	14.7	1.00	1.0	37.5	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
A		m1_core	M1 Core	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	kintex-7-3	James	Brakef	3456	6			233	##	14.7	1.00	1.0	67.3	verilog	9	m1_core		yes	N		4G	4G	Y		32		2007	2012		GCC target?	
A	1	m16c5x	SoC:M16C5x	mature	Michael Morris	PIC16	8	14	spartan-3-4	Michael	Morr	1265	4		3	60	##		0.33	1.0	15.7	verilog	3	m16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets	SOC LUT count	core at P16C5X
B		m65		stable	Naohiko Shimizu	6502	8	8x	arria-2	James	Brakef	483	A			110	##	q13.1	0.33	4.0	18.8	sfl & TDF	8	m65cpu	yes	yes	N	N	4K	4K	Y				2001	2002	6502 data sheets		
A		m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3	Michael	Morr	661	4		3	74			0.33	4.0	9.2	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
A		m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-3-5	James	Brakefield		4		3		##	14.7	0.33	4.0		verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
A	1	m65c02	M65C02	mature	Michael Morris	6502	8	8x	spartan-6-3	James	Brakef	466	6		3	118	##	14.7	0.33	4.0	20.8	verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
A		m65c02	M65C02	mature	Michael Morris	6502	8	8x	kintex-7-3	James	Brakef	661	6		3		##	14.7	0.33	4.0		verilog	13	M65C02	yes	yes	N	N	64K	64K	Y				2013	2014	6502 data sheets		
X		manik		stable	Sandeeo Dytta	RISC	32	32	kintex-7-3	James	needs editing		6					14.7	0.33	1.0		vhdl	45	manik2to	yes	yes	N		4K	4K	Y		16		2002	2006	www.niktech.com/	optional data & inst caches	supports Xilinx, Altera, Actel, Lattice
X	1	marca	McAdam's RISC (	stable	Wolfgang Puffitsch	RISC	16	16	arria-2	James	Brakef	1763	A		22	157	##	q13.1	0.67	6.0	10.0	vhdl	40	marca	yes		N		8K	16K		75	16	4	2007	2009		serial multiply & divide	clks/inst is approx
A		mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	cyclone-2	James	Brakef	1250	4		3	88	##	q11.1	1.00	1.0	70.8	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data shee	not all instructions implemented	
A		mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	cyclone-4	James	Brakef	1255	4		3	115	##	q13.1	1.00	1.0	91.4	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data shee	not all instructions implemented	
A		mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	arria-2	James	Brakef	784	A		3	183	##	q13.1	1.00	1.0	232.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data shee	not all instructions implemented	
A		mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	spartan-3-5	James	Brakef	1367	4		3	80	##	14.7	1.00	1.0	58.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data shee	not all instructions implemented	moved everything to work library
A		mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	spartan-6-3	James	Brakef	911	6		2	114	##	14.7	1.00	1.0	125.3	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data shee	not all instructions implemented	moved everything to work library
A	1	mblite	MB-Lite	beta	Tamar Kranenburg	uBlaze	32	32	kintex-7-3	James	Brakef	941	6		2	227	##	14.7	1.00	1.0	240.9	vhdl	18	core_wb	yes	yes	N		4G	4G	Y	86	32		2009	2012	microBlaze data shee	not all instructions implemented	moved everything to work library
B		mc6809e		beta	Flint Weller	6809	8	8x	kintex-7-3	James	gate level prir		6					14.7	0.33	3.0		vhdl	26	core_680	yes	yes	N	N	64K	64K	Y				1999		6809 data sheets	course work, ASIC orientation	
A	1	mc8051		stable	Helmut Mayrhofer	8051	8	8x	kintex-7-3	James	Brakef	3022	6	1		83	##	14.7	0.33	4.0	2.3	vhdl	49	mc8051c	yes	yes	N	N	256	64K	Y				1999	2013	www.oreganosystems	fast 8051, version available with floating-point by David Lundgren	
X	1	mcpu	MCPU A minima	stable	Tim Boscke	accum	8	8	spartan-6-3	James	Brakef	41	6			384	##	14.7	0.08	1.0	749.0	vhdl	1	tb02cpu2	yes	asm	N		64	64	Y	4			2007	2014		fits into 32 macrocell CPLD	reduced MIPS/clk due to only 4 inst
	1	mcs-4	4004 CPU & MCS	alpha	Reece Pollack	4004	4	4	kintex-7-3	James	Brakef	228	6			376	##	14.7	0.16	4.0	66.0	verilog	7	i4004			N		4K	4K	N				2012	2012	4004 data sheets	4004 was multi-chip	clks/inst is approx
		mcu8	8-bit microcontr	sim?	Dimo Pepelyashev		8															vhdl	16	processor_E	asm												asm, simulated	
X	1	micro8a		beta	John Kent	accum	8	16	kintex-7	James	Brakef	531	6			204	##	14.7	0.33	3.0	42.3	vhdl	11	Micro8	yes		N	N	2K	2K	Y				2002	2002	members.optushome	derived from Tim Boscke's mcpu, not perfected	
X	1	micro16b		beta	John Kent	accum	16	16	kintex-7	James	Brakef	205	6			434	##	14.7	0.33	2.0	349.0	vhdl	1	u16bcpu	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome	very limited inst set	MIPS/clk adj'd, 2 clks/inst

	_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
	micro16b		beta	John Kent	accum	16	16	spartan-3E-	James Brakef		467	4		3	76	##	14.7	0.33	2.0	26.9	vhdl	13	Micro16b	yes	asm	N	N	64K	4K	Y	8			2002	2008	members.optushome	SOC version, very limited inst set	MIPS/clk adj'd, 2 clks/inst
A	microblaze		proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		1201	6		32	408			1.30	1.0	441.4	not avail			yes	yes	opt		4G	4G	Y	86	32	5	2002		www.xilinx.com/tools	performance optimized	70 configuration options, MMU optional
A	1 microblaze		proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546	6		1	320			1.03	1.0	603.7	not avail			yes	yes	opt		4G	4G	Y	86	32	3	2002		www.xilinx.com/tools	MicroBlaze MCS, smallest configuratio	70 configuration options, MMU optional
W	microcore		beta	Klaus Schleisiek	forth	32	8	spartan-6-3	James Brakef		591	6		1	71	##	14.7	1.00	1.0	120.1	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/de	AKA uCore110
W	1 microcore		beta	Klaus Schleisiek	forth	32	8	kintex-7-3	James Brakef		644	6			149	##	14.7	1.00	1.0	231.3	vhdl	10	core	yes	asm	N	Y	2M	512K					2004		has several PDFs	indexing into return stack, auto inc/de	AKA uCore110
	microriscii	MicroRISC II	alpha	Alikat	RISC	32	32														verilog	7	?			N		64K	64K	Y		16	5	2002	2009		very little code	
A	1 minimips	miniMIPS	stable	Poppy etal	MIPS	32	32	kintex-7-3	James Brakef		2939	6	8		118	##	14.7	1.00	1.0	40.1	vhdl	12	minimips	yes	yes	N		4G	4G	Y		32	5			MIPS I		
A	1 minirisc	Mini-Risc core	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf Usseln		460	4			80			0.33	1.0	57.4	verilog	7	risc_core	yes	yes	N	Y	256	4K	Y				2001	2012	PIC16 data sheets		
	minsoc	*minsoc*	stable	Raul Fajardo etal	OpenRISC	32	32	cyclone-2	James Brakef		4721	4	4	44	48	##	q11.1	1.00	1.0	10.2	verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
	minsoc	*minsoc*	stable	Raul Fajardo etal	OpenRISC	32	32	arria-2	James	failed in fitter	A					##	q13.1	1.00	1.0		verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
	minsoc	*minsoc*	stable	Raul Fajardo etal	OpenRISC	32	32	spartan-6-3	James	too many los	6	4	13			##	14.7	1.00	1.0		verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
W	1 minsoc	*minsoc*	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakef		4945	6	4	8	107	##	14.7	1.00	1.0	21.7	verilog	88	or1200_t	yes	yes	Y	M	4G	4G	Y		32		2009	2013	www.minsoc.com	minimal OR1200, vendor neutral, has caches	
B	mips_16	Educational 16-b	stable	Doyya Doyya	RISC	16	16	kintex-7-3	James	collapsed in c	6						14.7	1.00	1.0		verilog	12	mips_16	yes		N		64K	64K		13	8	5	2012	2012			
	mips_enhanc	MIPS_enhanced	stable	Lazaridis Dimitris, Ioan	SPARC	32	32												1.0		vhdl		leon3mp	yes	yes	N		4G	4G	Y		32		2010	2011	tar file does not matc	based on mips789, added cache?? Only	source is for Leon3
A	mips_fault_to	Mips-FaultTolera	stable	Lazaridis	MIPS	32	32												1.0		vhdl			yes	yes	N		4G	4G	Y		32		2013		MIPS data sheets	arithmetic includes fault detection	
	mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	cyclone-2	James Brakef		6843	4	8		45	##	q11.1	1.00	1.0	6.6	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
A	mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	cyclone-4	James Brakef		9556	4			48	##	q13.1	1.00	1.0	5.0	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	did not infer multipliers
A	1 mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	arria-2	James Brakef		3716	A	8		79	##	q13.1	1.00	1.0	21.3	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
A	mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	spartan-3-5	James Brakef		6322	4	8		38	##	14.7	1.00	1.0	6.0	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
A	mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	spartan-6-3	James Brakef		4823	6	8		43	##	14.7	1.00	1.0	8.8	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
A	mips32r1	MIPS32 Release	stable	Grant Ayers	MIPS	32	32	kintex-7-3	James Brakef		4822	6	8		90	##	14.7	1.00	1.0	18.6	verilog	20	processor	yes	yes	N		4G	4G	Y		32		2012	2014	MIPS data sheets	Harvard arch	
A	1 mipsr2000	mipsr2000	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakef		1971	6	4	6	71	##	14.7	1.00	1.0	36.2	vhdl	35	Dm	yes	yes	N		4G	4G	Y		32	5	2012	2013	MIPS data sheets	course project	
A	1 mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakef		1432	6		1	171	##	14.7	1.00	1.0	119.1	verilog	10	mips_cor	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
A	1 mips789	mips789	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakef		1432	6		1	171	##	14.7	1.00	1.0	119.1	verilog	10	mips_cor	yes	yes	N		4G	4G	Y		32		2007	2009	MIPS data sheets		
	mproz		stable		RISC	16	16														schematic			yes	asm	N			32K					1999			little documentation, CPLD implementation	
	mpx	MPX 32-bit CPU	stable	Ultra Embedded		32	32														verilog					N		4G	4G	Y		32		2012	2013		GCC tools, no Verilog	
X	1 msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James Brakef		303	6			256	##	14.7	0.67	1.0	566.4	vhdl	13	cpu	yes	asm	N		256			16			2001			CPLD prototype	
A	myblaze	myBlaze	mature	Jian Luo	uBlaze	32	32												1.0		myhdl			yes	yes	N		4G	4G	Y		32		2010	2010	microBlaze data shee	clone, python code generators	
W	myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SP-spartan-	James Brakef		4494	4		12	67	##	14.7	1.00	1.0	15.0	vhdl	3	theCore	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis,	four variants
W	myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SP-kintex7-	James Brakef		2959	6		6	223	##	14.7	1.00	1.0	75.3	vhdl	3	theCore	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis,	four variants
W	myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SP-spartan-	Gerhard Hoh		6526	4		14	60	##	i9.2	1.00	1.0	9.2	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis	8.32 Whetstones
W	myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SPC-spartar	Gerhard Hoh		8134	4		17	61	##	i9.2	1.00	1.0	7.4	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis	7.32 Whetstones
W	1 myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SPM-sparta	Gerhard Hoh		7275	4	16	14	68	##	i9.2	1.00	1.0	9.3	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis	25.15 Whetstones
W	myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SPMC-spart	Gerhard Hoh		9499	4	16	17	53	##	i9.2	1.00	1.0	5.6	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis	2.02 Whetstones
W	myforthproce	FORTH processo	stable	Gerhard Hohner	forth	32	8	SPMD-spart	Gerhard Hoh		9265	4	16	14	63	##	i9.2	1.00	1.0	6.8	vhdl	58	mycpu	yes	yes	N		64M	64M		96			2004	2012		DPANS'94 32-bit Forth, masters thesis	22.5 Whetstones
X	myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-2	Muza	Altera	186	4		2	57			0.33	1.0	101.2	verilog	1	myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
X	myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-2	James Brakef		182	4		2	93	##	q11.1	0.33	1.0	169.0	verilog	1	myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
X	myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	cyclone-4	James Brakef		198	4		2	128	##	q13.1	0.33	1.0	212.9	verilog	1	myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
X	1 myrisc1	myRISC1	stable	Muza Byte	RISC	8	8	arria-2	James Brakef		121	A		2	231	##	q13.1	0.33	1.0	628.7	verilog	1	myRISC1	yes		N	Y	256	256	Y	16	4		2011	2011		Verilog source included in PDF file	LPM macros
W	natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	spartan-3e-	James Brakef		385	4		2	59	##	14.7	0.11	3.0	5.7	verilog	12	natalius_t	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
W	1 natalius_8bit	Natalius 8 bit RIS	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakef		232	6		1	175	##	14.7	0.11	3.0	27.7	verilog	12	natalius_t	yes	asm	N	Y	256	2K	Y	29	8		2012	2012		return stack & register file	3 clocks/inst
A	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-2	James Brakef		1567	4			74	##	q11.1	0.33	1.0	15.6	verilog	1	softusb_n	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-4-6	James Brakef		1561	4			102	##	q13.1	0.33	1.0	21.5	verilog	1	softusb_n	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	cyclone-5	James Brakef		1566	A			103	##	q13.1	0.33	1.0	21.8	verilog	1	softusb_n	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	arria-2	James Brakef		1126	A			154	##	q13.1	0.33	1.0	45.1	verilog	1	softusb_n	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	spartan-3-5	James	internal error	4					##	14.7	0.33	1.0		verilog	1	softusb_n	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	spartan-6-3	James Brakef		1038	6			116	##	14.7	0.33	1.0	36.9	verilog	1	softusb_n	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	1 navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	kintex-7-3	James Brakef		990	6			207	##	14.7	0.33	1.0	69.0	verilog	1	softusb_n	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
A	navre	Navre AVR clone	stable	Sebastien Bourdeaudu	AVR	8	16	ecp-3-6	James Brakef		1338	4			40	##	3.1	0.33	1.0	9.8	verilog	1	softusb_n	yes	yes	N		64K	64K	Y		32	2	2010	2013	AVR data sheets	AVR clone, part of www.milkymist.org	
	ncore	nCore	alpha	Stefan Istvan	RISC	8	8														verilog	3	nCore	yes		N					16	16		2006	2009			
	neptune-core	The Neptune Co	planning	Llama																	no source													2003	2009		single schematic	
A	next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-2	James Brakef		2865	4	1		39	##	q11.1	0.67	2.0	4.6	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
A	next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-4	James Brakef		3252	4			48	##	q13.1	0.67	2.0	4.9	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	did not infer multiplier
A	next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	cyclone-5	James Brakef		2710	A	1		44	##	q13.1	0.67	2.0	5.4	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
A	1 next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	arria-2	James Brakef		1966	A	2		77	##	q13.1	0.67	2.0	13.1	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
A	next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	spartan-3-5	James Brakef		2763	4	1		34	##	14.7	0.67	2.0	4.2	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
A	next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	spartan-6-3	James Brakef		2716	6	1		44	##	14.7	0.67	2.0	5.4	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
A	next186	Next 80186 proc	stable	Nicolae Dumitrache	8086	16	8x	kintex-7-3	James Brakef		2500	6	1		94	##	14.7	0.67	2.0	12.6	verilog	4	Next186_	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	boots DOS	
	next186_soc	Next186 SoC PC	stable	Nicolae Dumitrache	8086	16	8x	spartan-3a-	James	translate erro	4	1				##	14.7	0.67	2.0		verilog	14	ddr_186	yes	yes	N	N	1M	1M	Y				2013	2014	x86 data sheets	SoC version of next186	boots DOS
	next186_soc	Next186 SoC PC	stable	Nicolae Dumitrache	8086	16	8x	kintex-7-3	James	translate erro	6	1				##	14.7	0.67	2.0		verilog	14	ddr_186	yes	yes	N	N	1M	1M	Y				2013	2014	x86 data sheets	SoC version of next186	boots DOS
A	1 nextz80	NextZ80	stable	Nicolae Dumitrache	Z80	8	8x	kintex-7-3	James Brakef		1064	6			106	##	14.7	0.33	3.0	10.9	verilog	3	NextZ80C	yes	yes	N	N	64K	64K	Y				2011	2014	z80 data sheets		
W	1 nige_machine		stable	Andrew Read	forth	32	8	kintex-7-3	James Brakef		5033	6	8	33	123	##	14.7	1.00	1.0	24.5	vhdl	29	Board	yes	yes	N		16M	16M		512	512			2014			standalone Forth system	
	nige_machine		stable	Andrew Read	forth	32	8	kintex-7-3	James	too m	3381	6	8	1		##	14.7	1.00	1.0		vhdl	29	CPU	yes	yes	N		16M	16M		512	512			2014			standalone Forth system	
A	nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		2065	4			160			1.13	1.0	87.2	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
A	nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1355	A			170			1.13	1.0	141.1	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
A	nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1050	A			160			1.13	1.0	171.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
A	nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1355	A			280			1.13	1.0	232.5	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
A	1 nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		895	A			310			1.13	1.0	389.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II/f: fastest version
A	nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1915	4			130			0.64	1.0	43.2	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
A	nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		1045	A			170			0.64	1.0	103.4	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Hazd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
A		nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		1570	A			140			0.64	1.0	56.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
A		nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		1045	A			250			0.64	1.0	152.1	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
A		nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		1300	A			300			0.64	1.0	146.7	not avail			yes	yes	opt		4G	4G	Y		32		2004		NIOS2 data sheets	fltg-pt, caches & MMU options	Nios II: balanced version
A		nios2		proprietar	Altera	Nios II	32	32	cyclone-4-6	Altera		1080	4			170			0.15	1.0	23.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
A		nios2		proprietar	Altera	Nios II	32	32	arria-2	Altera		730	A			300			0.15	1.0	61.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
A		nios2		proprietar	Altera	Nios II	32	32	cyclone-5	Altera		840	A			200			0.15	1.0	35.7	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
A		nios2		proprietar	Altera	Nios II	32	32	arria-5	Altera		730	A			320			0.15	1.0	65.8	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
A		nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera		445	A			340			0.15	1.0	114.6	not avail			yes	yes	N		4G	4G	Y		32		2004		NIOS2 data sheets	serial arithmetic	Nios II/e: minimum LUTs version
A	1	oc54x	OpenCores54x D	beta	Richard Herveille	DSP	16	16	kintex-7-3	James	Brakef	2225	6	1		180	##	14.7	0.67	1.0	54.1	verilog	10	oc54_cpu	yes	yes	N	Y	64K	64K					2002	2009		40-bit accumulator, barrel shifter	C54x clone
W	1	octavo		beta	Charles LaForest	reg	16	16	stratix-4	Charles	LaFor	500	A	1		550			0.67	1.0	737.0	verilog	18	Octavo	yes	asm	N					14	16	10		2012	Octavo: an FPGA-Cen	8 core barrel, adjustable data width	~= performance across word sizes, no call/rtn ir
B		oks8	oks8	alpha	Kongzilee	ARM7	32	32	kintex-7-3	James	bad coding pr		6				##	14.7	0.67	1.0		verilog	8	oks8	yes	yes	N		64K	64K	Y				2006	2009		clone of KS86C4204/C4208/P4208, SAM87RI instruction set	
		oops	OoOPs Out-of-O	planning	Joshua Smith	MIPS	32	32														verilog	13		yes	yes	N		4G	4G	Y		32		2012	2012		incomplete source code	
W	1	open8_urisc	Open8 uRISC	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James	Brakef	691	6	1		263	##	14.7	0.33	1.0	125.6	vhdl	9	Open8	yes	yes	N		64K	64K	Y		8		2006	2013		accum & 8 regs, clone of Vautomation uRISC processor, in use	
		opencpu32	OpenCPU32	planning	Leonardo Araujo dos Dantos		32	32														vhdl	22	pkgOpenCPU32			N					16		2012	2012		built to test division algorithms	
		openfire_core	OpenFire Proces	alpha	Alex Marschner, Steph	uBlaze	32	32	kintex-7-3	James	empty project		6					14.7	0.33	1.0		verilog	12	openfire_	yes	yes	N	N	4G	4G	Y		32		2007	2009	uBlaze data sheets	"FPGA Proven"	
A		openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	spartan-3-5	James	Brakef	1352	4	3	6	39	##	14.7	1.00	1.0	28.8	verilog	27	openfire_	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's OpenFire
A	1	openfire2	OpenFIRE	beta	Antonio Anton	uBlaze	32	32	kintex-7-3	James	Brakef	1201	6	3	2	105	##	14.7	1.00	1.0	87.4	verilog	27	openfire_	yes	yes	N	N	4G	4G	Y		32		2007	2012	uBlaze data sheets	"FPGA Proven"	derived from Stephen Craven's OpenFire
A		openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	cyclone-4-6	Oliver	Girard	1750	4	1		52			0.67	2.0	9.9	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
A	1	openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	stratix-3-2	Oliver	Girard	1147	A	1		98			0.67	2.0	28.5	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
A		openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	spartan-6-4	Oliver	Girard	1424	6	1		68			0.67	2.0	15.9	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
A		openmsp430	*openMSP430*	stable	Oliver Girard	msp430	16	16x	virtex-6-3	Oliver	Girard	1387	6	1		116			0.67	2.0	27.9	verilog	30	openMSP	yes	yes	N	N	64K	64K	Y		16		2009	2014	msp430 data sheets	performance spreadsheet	
		or10		simulatior	R. Diez	OpenRISC	32	32											1.00	2.0		verilog	6	or10_top	yes	yes	N	M	4G	4G	Y		32		2012	2014		no longer maintained	
W		or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauc	1 slot	3663	6			72	##		1.00	1.0	19.7	verilog	39	or1200_ic	yes	yes	Y		4G	4G	Y		32		2010	2013		original version of OR1200	numbers from published paper
W		or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauc	2 slot	4535	6			136	##		1.00	1.0	30.1	verilog	39	or1200_t	yes	yes	Y		4G	4G	Y		32		2010	2013		2 slot barrel version of OR1200	numbers from published paper
W	1	or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauc	3 slot	5602	6			185	##		1.00	1.0	33.1	verilog	39	or1200_ic	yes	yes	Y		4G	4G	Y		32		2010	2013		3 slot barrel version of OR1200	numbers from published paper
W		or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauc	4 slot	6286	6			204	##		1.00	1.0	32.5	verilog	39	or1200_ic	yes	yes	Y		4G	4G	Y		32		2010	2013		4 slot barrel version of OR1200	numbers from published paper
		or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James	1 slot barrel		6					14.7	1.00	1.0		verilog	39	or1200_ic	yes	yes	Y		4G	4G	Y		32		2010	2013		original version of OR1200	
		or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James	2 slot	translat	6				##	14.7	1.00	1.0		verilog	39	or1200_t	yes	yes	Y		4G	4G	Y		32		2010	2013		2 slot barrel version of OR1200	
		or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James	3 slot barrel		6					14.7	1.00	1.0		verilog	39	or1200_ic	yes	yes	Y		4G	4G	Y		32		2010	2013		3 slot barrel version of OR1200	
		or1200_hp	OpenRisc 1200 H	stable	Strauch Tobias	OpenRISC	32	32	kintex-7-3	James	4 slot barrel		6					14.7	1.00	1.0		verilog	39	or1200_ic	yes	yes	Y		4G	4G	Y		32		2010	2013		4 slot barrel version of OR1200	
		or1200_soc	or1200_soc	beta	gaz	OpenRISC	32	32	cyclone-2	James	missing files		4				##	q11.1	0.67	2.0		verilog	39	top	yes	yes	Y		4G	4G	Y		32			2011		OpenRISC on Terasic DE1 board	
		or1200_soc	or1200_soc	beta	gaz	OpenRISC	32	32	arria-2	James	undefined ent		A				##	q13.1	0.67	2.0		verilog	39	top	yes	yes	Y		4G	4G	Y		32			2011		OpenRISC on Terasic DE1 board	
		or1200_soc	or1200_soc	beta	gaz	OpenRISC	32	32	kintex-7-3	James	unknown mod		6				##	14.7	1.00	1.0		verilog	39	top	yes	yes	Y		4G	4G	Y		32			2011		OpenRISC on Terasic DE1 board	
		or1k-cf	Confluence Oper	alpha	Kenr	OpenRISC	32	32														confluence													2004	2009			
W		or1k	OpenRISC	stable	Julius Baxter, Stefan Kr	OpenRISC	32	32	cyclcon-2	James	Brakef	3262	4	3	8	68	##	q11.1	1.00	1.0	20.9	verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
		or1k	OpenRISC	stable	Julius Baxter, Stefan Kr	OpenRISC	32	32	cyclcon-4	James	too many los		4				##	q13.1	1.00	1.0		verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
		or1k	OpenRISC	stable	Julius Baxter, Stefan Kr	OpenRISC	32	32	arria-2	James	failed in fitter		A				##	q13.1	1.00	1.0		verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
		or1k	OpenRISC	stable	Julius Baxter, Stefan Kr	OpenRISC	32	32	spartan-3-5	James	syntax errors		4				##	14.7	1.00	1.0		verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
W		or1k	OpenRISC	stable	Julius Baxter, Stefan Kr	OpenRISC	32	32	spartan-6-3	James	Brakef	3201	6	3	3	77	##	14.7	1.00	1.0	24.1	verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
W	1	or1k	OpenRISC	stable	Julius Baxter, Stefan Kr	OpenRISC	32	32	kintex-7-3	James	Brakef	3299	6	3	3	189	##	14.7	1.00	1.0	57.3	verilog	39	mor1kx	yes	yes	N	M	4G	4G	Y		32		2001	2014	http://opencores.org/	Cyclone IV board	cappuccino ALU
		or2k	OpenRISC 2000	planning	Marcus Erlandsson etal		32	32														no source																
		ourisc	16-bit Open uRIS	alpha	Joao Carlos		16	16	stratix-4	Joao	Carlos	500	A	1		550			0.67	1.0	737.0	vhdl										26			2013	2013		very incomplete source code	
X		p16		alpha	Don Golding	forth	16	5	kintex-7-3	James	bad syntax		6					14.7	0.67	1.0		vhdl	1	p16			N		64K	64K					2000				
A		p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	cyclone-2	James	Brakef	1216	4			87	##	q11.1	0.33	1.0	23.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
A		p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	cyclone-4	James	Brakef	1201	4			102	##	q13.1	0.33	1.0	27.9	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
A		p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	arria-2	James	Brakef	649	A			176	##	q13.1	0.33	1.0	89.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
A		p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-3-5	James	Brakef	487	4			90	##	14.7	0.33	1.0	60.7	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
A		p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	spartan-6-3	James	Brakef	352	6			133	##	14.7	0.33	1.0	124.2	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
A	1	p16c5x	P16C5x	mature	Michael Morris	PIC16	8	14	kintex-7-3	James	Brakef	378	6			252	##	14.7	0.33	1.0	220.2	verilog	3	P16C5x	yes	yes	N	Y	256	4K	Y				2013	2014	PIC16 data sheets		
A	1	pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo	Kocik	177	4		1	117			0.33	2.0	109.1	verilog	18	pacoblaze	yes	asm	N		256	2K	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
		pacoBlaze		mature	Pablo Kocik	picoBlaze	8	18	kintex-7-3	James	empty project		6					14.7	0.33	2.0		verilog	18	pacoblaze	yes	asm	N		256	2K	Y	57		2		2006	bleyer.org/pacoblaze	3 versions, behavioral coding	
		pavr	pAVR	alpha	Doru Cuturela	AVR	8	16														vhdl	8		yes	yes	N		64K	64K	Y		32	6	2003	2009	AVR data sheets	simulation only, is ASIC project	
A	1	pdp1	PDP-1 reimplem	alpha	Yann Vernier	PDP1	18	18	spartan-3a-	James	Brakef	1390	4		6	138	##	14.7	0.50	10.0	5.0	vhdl		top	yes	yes	N	N	4K	4K		28			2011	2011	http://pdp-1.compute	PDP-1 descended from MIT TX-0	uses Minimal UART from opencores
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	cyclone-2	James	Brakef	3340	4			50	##	q11.1	0.67	2.0	5.0	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.h
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	cyclone-4	James	Brakef	3439	4			64	##	q13.1	0.67	2.0	6.2	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.h
A	1	pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	arria-2	James	Brakef	2532	A			126	##	q13.1	0.67	2.0	16.7	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.h
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	spartan-3-5	James	Brakef	3842	4			56	##	14.7	0.67	2.0	4.8	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.h
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	spartan-6-3	James	Brakef	2966	6			64	##	14.7	0.67	2.0	7.3	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.h
A		pdp11-34verilog		stable	Brad Parker	PDP11	16	16x	kintex-7-3	James	Brakef	3089	6			153	##	14.7	0.67	2.0	16.6	verilog	24	pdp11	yes	yes	N	N	64K	64K			8		2009		PDP11 data sheets	boots & runs RT-11, EIS inst & MMU	www.heeltoe.com/download/pdp11/README.h
A		pdp2011		stable	Sytse van Slooten	PDP11	16	16x	arria-2	James	Brakef	4888	A	2	1	162	##	q13.1	0.67	2.0	11.1	vhdl	3	cpu	yes	yes	Y	Y	64K	64K			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/pdp-11/
A		pdp2011		stable	Sytse van Slooten	PDP11	16	16x	arria-2	James	Brakef	13221	A	2	14	35	##	q13.1	0.67	2.0	0.9	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/pdp-11/
A	1	pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James	Brakef	5060	6	1		205	##	14.7	0.67	2.0	13.6	vhdl	3	cpu	yes	yes	Y	N	64K	64K			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/pdp-11/
A		pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James	Brakef	13495	6	1	3	6	##	14.7	0.67	2.0	0.2	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/pdp-11/
A		pdp2011		stable	Sytse van Slooten	PDP11	16	16x	kintex-7-3	James	Brakef	13327	6	1		45	##	v14.1	0.67	2.0	1.1	vhdl	32	unibus	yes	yes	Y	N	4M	4M			8		2008	2014	PDP11 data sheets	SoC, build files for A&X boards	http://pdp2011.sytse.net/wordpress/pdp-11/
A		pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	spartan-6-3	James	Brakef	1332	6	1		81	##	14.7	0.50	2.0	15.1	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
A	1	pdp8	PDP-8 Processor	alpha	Joe Manojlovick, Rob D	PDP8	12	12	kintex-7-3	James	Brakef	1219	6	1		183	##	14.7	0.50	2.0	37.5	vhdl	55	cpu	yes	yes	N	N	32K	32K			8		2012	2013	PDP8 data sheets	Boots OS/8, runs apps, several variants	
A	1	pdp8l	Minimal PDP8/L	beta	Ian Schofield	PDP8	12	12	cyclone-3	James	Brakef	1088	4		48	63	##	q13.1	0.50	2.0	14.4	vhdl	11	top	yes	yes	N	N	4K	4K					2013		PDP8 data sheets		
A		pdp8verilog		stable	Brad Parker	PDP8	12	12	spartan-6-3	James	Brakef	509	6			162	##	14.7	0.50	2.0	79.5	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.ht
A	1	pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James	Brakef	505	6			366	##	14.7	0.50	2.0	181.3	verilog	18	pdp8	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.ht
A		pdp8verilog		stable	Brad Parker	PDP8	12	12	kintex-7-3	James	Brakef	1117	6			251	##	14.7	0.50	2.0	56.1	verilog	18	top	yes	yes	N	N	32K	32K			8		2005	2010	PDP8 data sheets	boots & runs TSS/8 & Basic	www.heeltoe.com/download/pdp8/README.ht

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
		pepelatz_mis	Pepelatz MISC	planning	Myname IsTeapot	MISC																verilog	1														insignificant source	
B	1	pic_coonan		alpha	Tom Coonan	PIC16	8	14	kintex-7-3	James Brakef		328	6		1	165	##	14.7	0.33	1.0	166.1	verilog	7	piccpu	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets		
A	1	picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	spartan-3-4	James Brakef		178	4			182	##	14.7	0.33	2.0	168.9	vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
A		picoblaze	picoblaze	stable	Ken Chapman	picoBlaze	8	18	kintex-7-3	James	ROM paramet		6				##	14.7	0.33	2.0		vhdl	1	kcspm3	yes	asm	N		256	2K	Y				2003		picoblaze data sheets	2 clocks per inst	this is the original picoBlaze author
A	1	plasma	Plasma most MI	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakef		2462	6		3	97	##	14.7	1.00	1.0	39.5	vhdl	22	plasma	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	wide outside use, opencores page has list of related publications	
X		popcorn		stable	Jeung Joon Lee	accum	8	8x	spartan-6-3	James Brakef		268	6			171	##	14.7	0.33	1.0	210.9	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
X	1	popcorn		stable	Jeung Joon Lee	accum	8	8x	kintex-7-3	James Brakef		267	6			347	##	14.7	0.33	1.0	428.4	verilog	4	pc	yes		N		64K	64K	Y	43			2000			small 8 bit uP	
A		ppx16	PPX16 mcu	stable	Daniel Wallner	PIC16	8	14	spartan-6-3	James	missing ROM BB							14.7		1.0		vhdl	10	P16C55, F	yes	yes	N	Y	256	4K	Y				2002	2009	PIC16 data sheets	both 16C55 & 16F84	
X	1	qrisc32	qrisc32 wishbon	alpha	Viacheslav	RISC	32	32	arria-2	James Brakef		3075	A	4		144	##	q13.1	1.00	1.0	46.9	system v	8	qrisc32	yes	yes	N		4G	4G	Y		32	4	2010	2011		for PhD thesis	
		r2000	r2000 Soc	alpha	Abdallah ElIbrahimi	RISC	32	32														verilog														empty tar file	
X		raptor64	Raptor64	planning	Robert Finch	RISC	64	32	kintex-7-3	James	missing port n		6					14.7	1.50	1.0		verilog	48	Raptor64	yes	yes	Y		2<<64	2<<64	Y		32		2012	2013		8-16-32-64 bit data, cache, MMU, hyper-threaded version also	
A		recore54		beta	ht-lab.com	PIC16	8	14	kintex-7-3	James	Cannot find <r		6					14.7	0.33	1.0		vhdl	20	rcore54_s	yes	yes	N	Y	256	4K	Y				1999		PIC16 data sheets	PIC16 clone	www.ht-lab.com
		risc_core_i	RISC_Core_I	planning	Manuel Imhof	RISC	16	16	kintex-7-3	James Brakef		349	6	1		717	##	14.7	0.67	1.0	1377.2	vhdl	13	CPU	yes	asm	N		1K	1K			8	4	2001	2009		Havard arch	dubious Fmax
X	1	risc0		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		1186	6	4	6	110	##	14.7	0.67	1.0	61.9	verilog	8	RISC0	yes	yes	N		4G	4G					2011			minimalist Wirth, education tool	
A	1	risc16f84	risc16f84	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakef		331	6			333	##	14.7	0.33	1.0	332.3	verilog	1	risc16f84	yes	yes	N	Y	256	4K	Y				2002	2013	PIC16 data sheets	derived from CQPIC by Sumio Morioka	
		risc5		beta	Niklaus Wirth	RISC	32	32	cyclone-2	James Brakef		3749	4		4	32	##	q11.1s	1.00	1.0	8.5	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Ober	32x32 multiplier
W		risc5		beta	Niklaus Wirth	RISC	32	32	cyclone-4	James Brakef		3503	4		1	54	##	q13.1	1.00	1.0	15.4	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Ober	32x32 multiplier ?
W		risc5		beta	Niklaus Wirth	RISC	32	32	arria-2	James Brakef		2362	A		3	73	##	q13.1	1.00	1.0	31.0	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Ober	32x32 multiplier
W		risc5		beta	Niklaus Wirth	RISC	32	32	spartan-3-5	James Brakef		3005	4	4	1	34	##	14.7	1.00	1.0	11.4	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Ober	32x32 multiplier
W		risc5		beta	Niklaus Wirth	RISC	32	32	spartan-6-3	James Brakef		2283	6	4	1	55	##	14.7	1.00	1.0	24.3	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Ober	32x32 multiplier
W	1	risc5		beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		2441	6	4	1	92	##	14.7	1.00	1.0	37.8	verilog	8	RISC5	yes	yes	Y		4G	4G			16		2013			minimalist Wirth, part of Project Ober	32x32 multiplier
A		risc5x	RISC5x	stable	MikeJ	PIC16	8	14	kintex-7-3	James	RLOC constrai		6					14.7	0.33	1.0		vhdl	15	cpu	yes	yes	N	Y	256	4K	Y				2002	2011	PIC16 data sheets	makes extensive use of xilinx primitives	
A		riscmcu	RISC Microcontr	stable	Yapzihe	AVR	8	16	arria-2	James	LPM paramet		6					14.7	0.33	1.0		vhdl	15	v_riscmcu	yes	yes	N		128	512	Y	92	16		2002	2009	AVR data sheets		
W		rise	RISE Microproce	beta	Jlechner etal	RISC	16	16	kintex-7-3	James	missing black		6	1				14.7	0.67	1.0		vhdl	26	rise	yes	asm	N		64K	64K			16	5	2006	2010	en.wikiversity.org/wik	ARM style register usage	
W		rtf65002	RTF65002	alpha	Robert Finch	accum	32	8x	kintex-7-3	James Brakef		13615	6	4	4	78	##	14.7	0.67	2.0	1.9	verilog	10	rtf65002c	yes		N		4G	4G	Y		16		2013	2013		32-bit 6502 + 6502 emulation	"proven"
W	1	rtf65002	RTF65002	alpha	Robert Finch	accum	32	8x	kintex-7-3	James Brakef		11216	6	4	6	111	##	v14.1	0.67	2.0	3.3	verilog	10	rtf65002c	yes		N		4G	4G	Y		16		2013	2013		32-bit 6502 + 6502 emulation	"proven"
B	1	rtf68ksys	rtf68kSys	alpha	Robert Finch	68000	16	16x	spartan-3e-	James	need t	13639	4	12	17		##	14.7	0.67	4.0		verilog	49	rtf68kSys	yes	yes	N	N	4G	4G	Y		16		2011	2011	68000 data sheets	based on Tobias Gubener's TG68	
B	1	rtf8088	rtf8088	planning	Robert Finch	8086	8x	8x	kintex-7-3	James Brakef		4514	6	4		174	##	14.7	0.67	3.0	8.6	verilog	57	rtf8088	yes	yes	N	N	1M	1M	Y				2012	2013	x86 data sheets	8-bit memory data, e.g. 8088	
		s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	arria-2	James	syntax errors		A				##	q13.1	2.00	1.0		verilog	136	s1_top	yes	yes	Y	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	
A		s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakef		54434	6	8	57	50	##	14.7	2.00	1.0	1.8	verilog	136	s1_top	yes	yes	Y	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	ISE run
A	1	s1_core	S1 Core	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakef		52845	6	8	59	56	##	v14.1	2.00	1.0	2.1	verilog	136	s1_top	yes	yes	Y	N	4G	4G	Y		32		2007	2012	SPARC data sheets	reduced version of OpenSPARC T1	Vivado run
W	1	sayeh_proces	SAYEH educatior	stable	Alireza Haghdoost, Arn	RISC	16	8x	kintex-7-3	James Brakef		479	6	1		164	##	14.7	0.67	1.0	229.7	verilog	13	Sayeh	yes		N		64K	64K			32		2008	2009	haghdoost.persiangig	simple RISC	
W		scarts	Scarts Processor	beta	Jlechner, Martin Walte	RISC	16	16	kintex-7-3	James	missing signal		6					14.7	0.67	1.0		vhdl	18	scarts		yes	N		64K	64K		122	16	4	2011	2012		GCC compiler	
A	1	secretblaze		beta	Lyonel Barthe	uBlaze	32	32	spartan-3-4	Lyonel Barthe		1563	4			91		i12.1	1.00	1.0	58.2	vhdl	26	sb_core		yes			4G	4G	Y	86	32	5	2010	2012	www.lirmm.fr/ADAC/		
A	1	socz80		stable	Will Sowerbutts	Z80	8	8x	spartan-6-3	James	constr	2568	6		15	93	##	14.7	0.33	3.0	4.0	vhdl	25	top_level	yes	yes	N	N	64K	64K	Y				2013	2014	z80 data sheets	based on Daniel Wallner's T80, for Par	http://sowerbutts.com/socz80/
A		socz80		stable	Will Sowerbutts	Z80	8	8x	kintex-7-3	James	source uses Sy		6		8		##	14.7	0.33	3.0		vhdl	25	top_level	yes	yes	N	N	64K	64K	Y				2013	2014	z80 data sheets	based on Daniel Wallner's T80, for Par	http://sowerbutts.com/socz80/
		sparcv8copro	Coprocessor-rea	planning	Nicholas Voorsanger	SPARC	32	32														no files												2012		SPARC data sheets		
W		ssbcc	Smal Stack Base	stable	Rodney Sinclair	forth	8	9	arria-2	James	syntax errors		A				##	q13.1	0.33	1.0		system v	3	core	yes	asm	N								2012	2014		Python program generates the Verilog	
A		storm_core	Storm Core (ARN	beta	Stephan Nolting	ARM7	32	32	cyclone-2-6	Stephan Nolt		11469	4	3	75	179			1.00	1.0	15.6	vhdl	16	STORM_T	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
A		storm_core	Storm Core (ARN	beta	Stephan Nolting	ARM7	32	32	cyclone-4-6	Stephan Nolt		11518	4	3	67	157			1.00	1.0	13.7	vhdl	16	STORM_T	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
A	1	storm_core	Storm Core (ARN	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef		2312	6	3		179	##	14.7	1.00	1.0	77.4	vhdl	16	CORE	yes	yes	N		4G	4G	Y		32	8	2011	2014		I & D caches not compiled	
A		storm_core	Storm Core (ARN	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef		3514	6	3	4	157	##	14.7	1.00	1.0	44.8	vhdl	16	STORM_T	yes	yes	N	M	4G	4G	Y		32	8	2011	2014		I & D caches	
		sub86	Small x86 subset	alpha	Jose Rissetto	8086	8x	8x														verilog	1	sub86	yes	yes	N	N	64K	64K	Y		7		2012	2013		no segment registers, limited op-codes	
W		sxp	SXP (Simple eXte	beta	Sam Gladstone etal	RISC	32	32			too many Ios											verilog		sxp			N		4G	4G			32		2001	2009		basic RISC	too many Ios
		suska-III		beta	Wolfgang Forster	68000	16	16x	cyclone-4-6	James Brakef		9894	4			34	##	q13.1	0.67	4.0	0.6	vhdl	11	wf68k00il	yes	yes	N	N	4G	4G	Y		16		2003	2013	68000 data sheets	for use as an Atari ST	http://www.experiment-s.de/en/
A	1	suska-III		beta	Wolfgang Forster	68000	16	16x	arria-2	James Brakef		7388	A			55	##	q13.1	0.67	4.0	1.3	vhdl	11	wf68k00il	yes	yes	N	N	4G	4G	Y		16		2003	2013	68000 data sheets	for use as an Atari ST	http://www.experiment-s.de/en/
A		synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	cyclone-2-6	James	ROM s	1436	4		1	76	##	q11.1s	0.33	1.0	17.5	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCORES/SYNPI
A		synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	cyclone-4-6	James	ROM s	1417	4		1	96	##	q13.1	0.33	1.0	22.4	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCORES/SYNPI
A		synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	arria-2	James	ROM s	1098	A			154	##	q13.1	0.33	1.0	46.2	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCORES/SYNPI
A		synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	spartan-3-5	James Brakef		805	4		1	58	##	14.7	0.33	1.0	23.8	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCORES/SYNPI
A		synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	spartan-6-3	James Brakef		517	6		1	89	##	14.7	0.33	1.0	57.0	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCORES/SYNPI
A	1	synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	kintex-7-3	James Brakef		474	6		1	197	##	14.7	0.33	1.0	136.8	vhdl	7	synpic12	yes	yes	N	N	256	2K	Y				2011	2011	PIC12 data sheets	CHDL to verilog	http://projects.nbee.es/display/IPCORES/SYNPI
A	1	system05	SOC:system05	beta	John Kent	6805	8	8x	kintex-7-3	James Brakef		834	6			204	##	14.7	0.33	4.0	20.2	vhdl	10	System05	yes	yes	N	N	64K	64K	Y				2003	2009	6805 data sheets		
A		system09	SOC:system09	stable	John Kent	6809	8	8x	spartan-6-3	James Brakef		2127	6			64	##	14.7	0.33	3.0	3.3	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
A	1	system09	SOC:system09	stable	John Kent	6809	8	8x	kintex-7-3	James Brakef		1945	6			154	##	14.7	0.33	3.0	8.7	vhdl	40	cpu09l	yes	yes	N	N	64K	64K	Y				2003	2012	6809 data sheets	from John Kent web page	
A	1	system11		alpha	John Kent, David Burne	68HC11	8	8x	kintex-7-3	James Brakef		1218	6			153	##	14.7	0.33	4.0	10.3	vhdl	17	cpu11	yes	yes	N	N	64K	64K	Y				2003	2009	6811 data sheets	known bugs & untested instructions	
A	1	system68	System68	stable	John Kent, David Burne	6801	8	8x	spartan-3-5	James Brakef		2235	4		4	46	##	14.7	0.33	4.0	1.7	vhdl	21	cpu68	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets		
B	1	system6801	Wishbone Syster	stable	Michael L. Hasenfratz	6801	8	8x	cyclone-3	James Brakef		1507	4		3	73	##	14.7	0.33	4.0	4.0	vhdl	15	wb_cyclo	yes	yes	N	N	64K	64K	Y				2003	2009	6801 data sheets	based on John Kent's 6801	tested on Apex20K, Cyclone & Straix boards
A	1	t400	*T400 uControlle*	stable	Arnim Laeuger	COP400	4	8x	cyclone-1	Arnim Laeuge		583	4		2	59			0.17	4.0	4.3	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
A		t400	*T400 uControlle*	stable	Arnim Laeuger	COP400	4	8x	spartan-2	Arnim Laeuge		643	4		2	60			0.17	4.0	4.0	vhdl	53	t400_core	yes	asm	N		256	1K					2006	2009	COP400 data sheets	several variants	
A	1	t48	*T48 uController*	stable	Arnim Laeuger	MCS-48	8	8x	cyclone-1	Arnim Laeuge		738	4		1	59			0.33	4.0	6.6	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
A		t48	*T48 uController*	stable	Arnim Laeuger	MCS-48	8	8x	spartan-2	Arnim Laeuge		771	4		1	30			0.33	4.0	3.2	vhdl	70	t48_core	yes	asm	N		256	1K					2004	2009	MCS-48 data sheets	used in several projects	
A	1	t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakef		1942	6	1		147	##	14.7	0.33	4.0	6.2	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
A		t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	kintex-7-3	James Brakef		1921	6	1	2	127	##	14.7	0.33	4.0	5.5	vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	8052 SoC
A		t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	arria-2	James	proba	3049	6	1		111	##	q13.1	0.33	4.0	3.0	vhdl	17	T8032	yes	yes	N	N	64K	64K	Y				2002	2010	8032 data sheets	8052 & 8032	8032 SoC
A		t51	T51 mcu	stable	Andreas Voggeneder	8051	8	8x	arria-2	James	proba	4704	6	1	1	89	##	q13.1	0.33	4.0	1.6	vhdl	17	T8052	yes	yes	N	N	64K	64K	Y				2002	2010	8052 data sheets	8052 & 8032	8052 SoC
A		t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	cyclone-2	James Brakef		829	4			84	##	q11.1s	0.33	4.0	8.4	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
A		t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	cyclone-4	James Brakef		831	4			110	##	q13.1	0.33	4.0	10.9	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
A		t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	arria-2	James Brakef		617	A			190	##	q13.1	0.33	4.0	25.4	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
A		t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-3-5	James Brakef		923	4			83	##	14.7	0.33	4.0	7.5	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	

		_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
A		t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	spartan-6-3	James Brakef		725	6			128	##	14.7	0.33	4.0	14.5	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
A	1	t65	T65 CPU	stable	Daniel Wallner	6502	8	8x	kintex-7-3	James Brakef		575	6			291	##	14.7	0.33	4.0	41.7	vhdl	7	T65	yes	yes	N	N	64K	64K	Y				2002	2010	6502 data sheets	6502, 65C02 & 65C816; wide use	
A		t6507lp	T6507LP	beta	Gabriel Oshiro, Samuel	6502	8	8x	spartan-6-3	James	errors							14.7		4.0		verilog	22	t6507lp	yes	yes	N	N	64K	64K	Y				2009	2010	6502 data sheets	for use in ATARI 2600	
A		t80	T80 cpu	stable	Daniel Wallner	8080	8	8x	spartan-6-3	James	8080 r	958	6			95	##	14.7	0.33	9.0	3.6	vhdl	5	T8080se	yes	yes	N	N	64K	64K	Y				2002	2011	8080 data sheets	Z80, 8080 & gameboy inst sets, several usages	
		t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	arria-2	James	xilinx primitive		A				##	q13.1	0.33	3.0		vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
A		t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-3-5	James	Z80 m	1991	4			54	##	14.7	0.33	3.0	3.0	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
A		t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	spartan-6-3	James	Z80 m	1462	6			83	##	14.7	0.33	3.0	6.2	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
A	1	t80	T80 cpu	stable	Daniel Wallner	Z80	8	8x	kintex-7-3	James	Z80 m	1389	6			163	##	14.7	0.33	3.0	12.9	vhdl	5	T80a	yes	yes	N	N	64K	64K	Y				2002	2011	z80 data sheets	Z80, 8080 & gameboy inst sets, several usages	
A	1	tg68	TG68 execute 68	stable	Tobias Gubener	68000	16	16x	kintex-7-3	James Brakef		2331	6			44	##	14.7	0.67	4.0	3.2	vhdl	2	TG68_fas	yes	yes	N	N	4G	4G	Y		16		2007	2012	68000 data sheets	for use with Minimig	
X		theia_gpu	Theia: ray graphi	beta	Diego Valverde	GPU														1.0		verilog	32	Theia	yes	asm	N						12		2011	2012		multi-core, 3D rendering & shader	
W		tiny64	Tiny64	stable	Ulrich Riedel	RISC	64		kintex-7-3	James	bit length mis		6					14.7	1.00	1.0		vhdl	7	TinyX		asm	N		64K	64K		16	8		2004	2009		word size configurable from 32 to 64	
X		tiny8	tiny8	mature	Ulrich Riedel	CISC	8	8x			Flex10K design									1.0		ahdl & schematic				asm	N		64K	64K	Y				2002	2009		registers in RAM like TMS9900, uses Altera AHDL, megafunctions & schematic entry	
X		tinycpu	TinyCPU	alpha	Jordan Earls	RISC	8	16	kintex-7-3	James	bit len	1182	6			200	##	14.7	0.33	2.0	28.0	vhdl	10	top		asm	N	N	64K	64K			16		2012	2012			
X		tisc	Tiny Instruction S	beta	Vincent Crabtree	accum	8	8x	spartan-6-3	James Brakef		198	6			60	##	14.7	0.33	1.0	99.5	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
X	1	tisc	Tiny Instruction S	beta	Vincent Crabtree	accum	8	8x	kintex-7-3	James Brakef		195	6			87	##	14.7	0.33	1.0	147.1	vhdl	1	TISC			N		256	1K	Y		2		2009	2009		minimal accumulator machine	
		totalcpu	TotalCPU	alpha		RISC	12+	12														verilog											16		2007	2009		data width 12 bits and up, no data memory	
A		turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	cyclone-2	Dinesh Annay		5072	4			39			0.33	4.0	0.6	verilog	74	oc8051_t	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
A	1	turbo8051	turbo 8051	beta	Dinesh Annayya	8051	8	8x	kintex-7-3	James Brakef		1985	6	1		127	##	14.7	0.33	4.0	5.3	verilog	74	oc8051_t	yes	yes	N	N	64K	64K	Y				2011	2013	8051 data sheets	includes perpherials	
A		tv80	TV80	mature	Guy Hutchison, Howard	Z80	8	8x	cyclone-2	James Brakef		2148	4			63	##	q11.1	0.33	3.0	3.2	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A		tv80	TV80	mature	Guy Hutchison, Howard	Z80	8	8x	cyclone-4	James Brakef		2193	4			86	##	q13.1	0.33	3.0	4.3	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A		tv80	TV80	mature	Guy Hutchison, Howard	Z80	8	8x	arria-2	James Brakef		1413	A			139	##	q13.1	0.33	3.0	10.9	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A		tv80	TV80	mature	Guy Hutchison, Howard	Z80	8	8x	spartan-3-5	James Brakef		2095	4			54	##	14.7	0.33	3.0	2.9	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A		tv80	TV80	mature	Guy Hutchison, Howard	Z80	8	8x	spartan-6-3	James Brakef		1180	6			83	##	14.7	0.33	3.0	7.8	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A	1	tv80	TV80	mature	Guy Hutchison, Howard	Z80	8	8x	kintex-7-3	James Brakef		1207	6			182	##	14.7	0.33	3.0	16.6	verilog	6	tv80n	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Daniel Wallner's T80, ASIC implementations	
A	1	ucore	Ucore	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakef		2469	6		1	231	##	14.7	1.00	1.0	93.5	verilog	25	ucore	yes	yes	N		4G	4G	Y		32	6	2005	2010	MIPS data sheets	MMU & caches	
X	1	usimplez	MicroSimplez	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo Salvade		48	4			134		q9.1	0.17	1.0	475.9	vhdl	3	usimplez_cpu			N		512	512		8			2011		http://www-gti.det.u	part of university course, simplez+i4 h	MIPS/Mhz reduced due to few inst
A	1	v1_coldfire		stable	IPextreme	68000	16	16x	cyclone-3	freescale		5000	4			80			0.89	1.0	14.2				yes	yes	N	N	4G	4G	Y		16		2008		68000 data sheets	free for Cyclone III	http://www.ip-extreme.com/IP/coldfire_altera
X	1	vtach	VTACH Bell Labs	mature	Al Williams		13	12	spartan-3-4	James Brakef		557	4			71	##	14.7	0.50	1.0	64.1	verilog	16	vtach			N		256	256	Y				2013	2014		ISE project only, BCD arithmetic	
X		vtach	VTACH Bell Labs	mature	Al Williams		13	12	kintex-7-3	James	xilinx core prc		6					14.7	0.50	1.0		verilog	16	vtach			N		256	256	Y				2013	2014		ISE project only, BCD arithmetic	
A		w11	PDP-11/70 CPU (	alpha	Walter Mueller	PDP11	8	16x	spartan-6	Walter Muell		3418	6			80			0.67	2.0	7.8	vhdl	26	pdp11	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
A	1	w11	PDP-11/70 CPU (	alpha	Walter Mueller	PDP11	8	16x	kintex-7-3	James Brakef		1760	6	1	1	147	##	14.7	0.67	2.0	28.0	vhdl	118	pdp11_cc	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
A		w11	PDP-11/70 CPU (	alpha	Walter Mueller	PDP11	8	16x	kintex-7-3	James Brakef		3174	6	1	3	131	##	14.7	0.67	2.0	13.9	vhdl	133	sys_w11a	yes	yes	N	N	4M	4M	Y		8		2010	2013	PDP11 data sheets	Boots UNIX, has MMU & cache, retro project	
A	1	wb_z80	Wishbone High F	stable	Brewster Porcella	Z80	8	8x	kintex-7-3	James Brakef		2025	6			144	##	14.7	0.33	3.0	7.8	verilog	4	z80_core_	yes	yes	N	N	64K	64K	Y				2004	2012	z80 data sheets	derived from Guy Hutchison TV80	
		wb4pb	Software Aided \	stable	Stefan Fischer	picoBlaze	13	13														vhdl & v	10					Y							2010	2013	picoblaze data sheets	software addon for picoBlaze	
X		x32		stable	Sijmen Woutersen	forth	32	8	kintex-7-3	James	missing define		6				##	14.7	1.00	1.0		vhdl	32	core	yes	yes	N		4G	4G	Y				2006	2007		MS thesis, byte code, needs caches	
X		xproz		stable	Herbert Kleebauer	CISC	16	16x												1.0		schematic			yes	asm	N		64K	64K					1995			documentation in German	
W		xr16		stable	Jan Gray	RISC	16	16	spartan-2-5	Jan Gray		257	4		2	37			0.67	1.0	96.6	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R
W		xr16		stable	Jan Gray	RISC	16	16	spartan-2-5	Jan Gray		200	4		2	50			0.67	1.0	167.5	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	handcrafted FPGA layout
W		xr16		stable	Jan Gray	RISC	16	16	spartan-3-5	James Brakef		392	4			80	##	14.7	0.67	1.0	136.2	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
W		xr16		stable	Jan Gray	RISC	16	16	virtex-4	James Brakef		392	4			149	##	14.7	0.67	1.0	254.9	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
W		xr16		stable	Jan Gray	RISC	16	16	spartan-6-3	James Brakef		283	6			98	##	14.7	0.67	1.0	233.2	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, speed mode better
W		xr16		stable	Jan Gray	RISC	16	16	virtex-5-2	James Brakef		288	6			131	##	14.7	0.67	1.0	305.9	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
W	1	xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakef		273	6			263	##	14.7	0.67	1.0	644.8	verilog	4	xr16	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, speed mode better
		xr16		stable	Jan Gray	RISC	16	16	spartan-3-5	James Brakef		502	4			82	##	14.7	0.67	1.0	109.6	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
		xr16		stable	Jan Gray	RISC	16	16	virtex-4	James Brakef		511	4			154	##	14.7	0.67	1.0	201.5	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
		xr16		stable	Jan Gray	RISC	16	16	spartan-6-3	James Brakef		336	6			92	##	14.7	0.67	1.0	183.6	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
		xr16		stable	Jan Gray	RISC	16	16	virtex-5-2	James Brakef		369	6			136	##	14.7	0.67	1.0	247.8	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode better
		xr16		stable	Jan Gray	RISC	16	16	kintex-7-3	James Brakef		337	6			202	##	14.7	0.67	1.0	402.0	verilog	12	xsoc	yes		N		64K	64K			16		1999	2001		handcrafted instruction set	tool FPGA P&R, area mode vastly better
A		y80e	Y80e Z80/Z180 c	stable	Sergey Belyashov	Z80	8	8x	kintex-7-3	James	empty project		6					14.7	1.00	3.0		verilog	15	y80_top	yes	yes	N	N	64K	64K	Y				2013	2013	z80 data sheets	based on Y80 from "Microprocessor Design Using Verilog HDL" by Monte Dalryple	
A		yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	arria-2	James	map errors		A				##	q13.1	1.00	1.0		verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntations	
A		yacc	YACC Yet Anothe	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James	map e	2220	6	6			##	14.7	1.00	1.0		verilog	10	yacc2	yes	yes	N		4G	4G	Y		32	5	2005	2009	MIPS data sheets	derived from, but independent of plasma, xilinx & altera implemntations	
X		yasep		alpha	Yann Guidon	RISC	16	32	kintex-7-3	James	syntax errors		6					14.7	1.00	1.0		vhdl		microYAE	yes	asm	N			2K			16		2008	2014	www.yaesp.org	Java generated VHDL, revisions ongoir	funky web site
B		yellowstar	Yellow Star	stable	Charles Brej	MIPS	32	32			missing declarations											verilog	1	processor	yes	yes	N		4G	4G	Y		32		2001	2013	MIPS data sheets	MIPS R3000 clone, gate level dsgn	brej.org/yellow_star/
A		z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	cyclone-3	James Brakef		2831	4		22	82	##	q13.1	0.33	3.0	3.2	vhdl	19	top_de1	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	removed pin assignments
A	1	z80soc	Z80 System on C	stable	Ronivon Costa	Z80	8	8x	spartan-3e-	James Brakef		2474	4	2	19	78	##	14.7	0.33	3.0	3.4	vhdl	19	top_s3e	yes	yes	N	N	64K	64K	Y				2008	2010	z80 data sheets	based on Daniel Wallner's T80	
A	1	zet86	Zet The x86 (IA-3	alpha	Zeus Marmolejo	8086	16	8x	kintex-7-3	James Brakef		3642	6	1		68	##	14.7	0.67	2.0	6.2	verilog	32	fpga_zet_	yes	yes	N	N	1M	1M	Y				2008	2014	x86 data sheets	equivalent to 80186, boots MS-DOS	zet.aluzina.org/index.php/Zet_processor
W		zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-3	Oyvind Harbo		440	4			85			0.10	1.0	19.3	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	opensource.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
W		zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	spartan-6	Oyvind Harbo		1259	6			135			0.10	1.0	10.7	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	opensource.zylin.com	zpu4: 16 & 32 bit versions, code size 80% of ARM (thumb), low MIPs/MHz	
W	1	zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	kintex-7-3	James Brakef		1073	6	3		283	##	14.7	0.10	1.0	26.4	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	opensource.zylin.com	zpu4: 16 & 32 bit versions, code size 8	zpu4 core
W		zpu	ZPU the worlds s	stable	Oyvind Harboe	forth	32	8	kintex-7-3	James Brakef		1352	6	3		276	##	14.7	0.10	1.0	20.4	vhdl	23	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2009	opensource.zylin.com	zpu4: 16 & 32 bit versions, code size 8	zy2000 core
W		zpuino	SoC:ZPUino	alpha	Alvaro Lopes	forth	32	8	spartan-6	James	source code e		6				##	14.7	1.00	1.0		vhdl	8	zpu_core	yes	yes	N		4G	4G	Y	37			2008	2012	http://alvie.com/zpui	SoC version of modified ZPU	pipelined

126 # usable(beta, stable or mature): "A"(clones) & "W"(originals) 51 ## ## ## # adrs

14 65 "B" or "X" of limited interest **171 unique usable designs**

Web page DMIPS per clock cycle per core en.wikipedia.org/wiki/Instructions_p community.freescale. www.eembc.org/coremark/index.php

MIPS/MHz Pro-rating for data size:

1-bit	0.04				uP	MIPS		CoreMarks /MHz	MHz		guessed average clocks/inst
8-bit	0.33	**Silicon Area equivalents**			4004	0.10					
16-bit	0.67	LUTS/DSP48	16:1		6502	0.50		0.02	0.06		4
32-bit	1.00	LUTS/Block RAM	32:1		8051	0.01	DMIPS	0.08	0.24		1, 4 or 6

Following has DMIPS per clock for many microprocessors
http://en.wikipedia.org/wiki/Instructions_per_second

_uP_cores_test folder	opencores name	status	author	style / clone	data size	inst size	FPGA	reporter	comment	LUTs ALUT	LUT?	mults	blk ram	F max	date	tool ver	MIPS /clk	clks/ inst	KIPS /LUT	src code	# src files	top file	doc	tool chain	fltg pt	Ha vd	max data	max inst	byte adrs	# inst	# reg	pipe len	start year	last revis	reference	note worthy	comments
Under the assumption that the core is capable of one instuction per clock																								8080					0.17				0.25			9	
																								68K					0.10				0.15			4	
																								ARM Cortex A9					2.50	DMIPS			2.90	1000			
																								ARM Cortex M0					0.90	DMIPS			1.50	70			
																								ARM Cortex M3					1.25	DMIPS			2.17	25			
																								ARM7					0.90			0.74	2.04	600			
																								AVR					1.00			0.21	0.53	8			
																								AVR32									1.62	60			
																								BA21									2.44	400			
																								Coldfire									2.80	400			
																								Coldfire									0.77	150	Virtex-5	2	
																								HCS08								0.04	0.12			4	
																								HC11												4	
																								LEON3/Spartan-6									1.96	100			
																								MC6809					1.24			0.07	1.86			3	
																								MicroBlaze 3-stage					1.03				1.50				
																								MicroBlaze 5-stage					1.38				1.90	125			
																								MIPS32					1.51				2.28				
																								MSP430								0.40	1.20			2	
																								MSP430									1.10	25		2	
																								Nios II					0.64	DMIPS			0.93	200			
																								Nios II -e					0.15	DMIPS			0.25				
																								Nios II -f					1.13	DMIPS			1.60	200			
																								PIC16					0.25								
																								PIC18									0.04	40			
																								PIC24								0.72	1.86	40			
																								PIC32									3.45	80			
																								Super H-2									1.44	180			
																								VAX780					1.00	DMIPS			1.50		DMIPS # is by definition		
																								Z80					1.60			0.01	0.03			3	
																								eSi-1600									1.98				

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	used to indicate best KIPS/LUT for a given design, usually using fast FPGA family
_uP_cores_test folder	if opencores design is their folder name, otherwise my folder name
opencores name	
status	ASIC, planning, alpha, beta, stable, mature, proprietary
author	First Name, Last Name
style / clone	part number or "forth", RISC, accumulator, etc
data size	data memory word size
inst size	instruction size
FPGA	FPGA family for compile, place, route & timing, usually using fastest part grade
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALUT	4-LUT, 6-LUT, Altera ALUT, Actel Tile
LUT?	total number of LUTs or ALUTs used including route-thrus & otherwise unavailable
mults	total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up
blk RAM	total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up
Fmax	maximum primary clock speed from compile, place & route run without clock constraints
date	date of compile, place & route; serves to identify source version
tool ver	Altera (**Q**uartus), Xilinx (ISE, **V**ivado), Lattice Semiconductor(**D**iamond) or MicroSemi(**L**ibero) tool version number
MIPS /clk	prorated DMIPS per clock, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
src code	VHDL or Verilog or System Verilog or schematic or gates
# src files	number of source files for compile, place, route & timing
top file	top file for compile, place, route & timing run
doc	is documentation provided
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point
Ha vd	separate instruction and data memory(s), there can be more than one data memory, M for MMU & caches
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, somewhat subjective
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions
reference	web address or generic information (for clones)
note worthy	anything special about the design
comments	catchall