Small soft core uP Inventory

Opencore and other soft core processors — Only cores in the "usable" category included

Most Prolific Authors	©2014 James Brakefield	
John Kent	micro8a, micro16b, system05, system09, system11, system68	6
Daniel Wallner	ax8, ppx16, t65, t80 (8080 & z80)	5
Shawn Tan	ae18, aeMB, k68, DCPU16	4
Ulrich Riedel	68hc05, 68hc08, tiny64, tiny8	4
Robert Finch	rtf65002, rtf68ksys, rtf8088	3
Jose Ruiz	ion, light52, light8080	3
Lazaridis Dimitris	mips_fault_tolerant, mipsr2000, mips_enhanced	3

Most Clones	©2014 James Brakefield	
MIPS	ion, minimips, mips_fault_tolerant, misp32r1, misp789, mipsr2000, plasma, ucore, yacc, m1_core	10
6502	ag_6502, cpu6502_true_cycle, free6502, lattice6502, m65c02, t65, t6507lp, m65	8
PIC16	free_risc8, lwrisc, minirisc, m16c5x, ppx16, recore54, risc16f84, risc5x	8
microblaze	aeMB, mblite, microblaze, myblaze, openfire_core, secretblaze	6
6800	hd63701, system68, system05, 68hc05, 68hc08	5
8051	dalton_8051, light52, mc8051, t51, turbo8051	5
avr	avr_core, avr_hp, avr8, navre, riscmcu	5
z80	nextz80, t80, tv80, wb_z80, y80e	5
openrisc	altor32, minsoc, or1k, or1200_hp	4
6809	6809_6309, system09, mc6809e	3
8080	cpu8080, light8080, t80	3
68000	ao68000, tg68, v1_coldfire	3
PDP-8	pdp8, pdp8l, pdp8verilog	3
picoblaze	copyblaze, pacoblaze, picoblaze	3

Most Numerous Original Processor Type	©2014 James Brakefield	
RISC	alwcpu, atlas_core, ba22, dcpu16, erp, gumnut, jane_nn, jpu16, latticemicro32, latticemicro8, natalius_8bit_risc, open8_risc, rise, sayeh_processor, scarts, szp, tiny64, xr16, cole_c16, diogenes, dragonfly, eco32, edge, eight_bit_uc, erp, fpgammix, hicovec, hpc-16, jam, manik, marca, myrosc1, raptor64, risc0, risc5, yasep	35
forth	b16, dfp, J1, jop, microcore, myforthprocessor, nige_machine, ssbcc, zpu, 8bit_chapman, cpu16, dataflow_chapman, msl16, p16, x32	15
accumulator	blue, lem1_9, leros, mcpu, popcorn, tisc, usimplez	11
other	lutiac, hive, c16, ensilica, octavo, lemberg, vtach, bobcat	8
openrisc	altor32, minsoc, mor1kx, or1k, or1200_hp	5

Usage beyond original author	©2014 James Brakefield	
amber	Amber ARM-compatible core	OCCP
leon	SPARC clone, commerical product, 50 FPGA boards supported	
minsoc	OpenRISC implementation of OR1200 SOC	OCCP
openMSP430	Clone of Texas Instruments MSP430 family	OCCP
or1k	OpenRISC 1000	OCCP
plasma	Plasma - most MIPS I opcodes	OCCP
system09	Color Computer, arcade games, SWTPC	
t400	T400 uController	OCCP
t48	T48 uController	OCCP
t80	8080, Z80 & gameboy inst sets; several usages	
zpu	Zylin CPU, commercial product	

Commercial product	©2014 James Brakefield	Known For
Synopsys ARC	Targets ASIC designs, very little public information	CAD tools
ARM Cortex A9	Incorporated into Altera Cyclone V and Xilinx Zynq	uP IP
ARM Cortex M3	Incorporated into MicroSemi SmartFusion1 & 2	uP IP

ARM Cortex M0	Targets FPGAs and very low cost 32-bit processors	uP IP
BA21-25	32-bit RISCs by CAST Inc., targets ASICs	IP
ColdFire	68000 clone by ip-extreme, free for Altera Cyclone 3	IP
Eric-5	Entner Electronics, 9-bit Forth	FPGA design
ESi-1600, Esi-3200	Ensilica 16-bit & 32-bit , targets both FPGAs & ASICs	design services
LEON	SPARC clone from Aeroflex Gaisler, LEON 2 & 3 source is free	SPARC IP
Manik	32-bit RISC, Nitech core, free source	design services
MC8051	8051 clone from Oregano Systems, source is free	design services
Micro 8 & 32	8 & 32-bit Lattice cores, originally open source, now bundled with free Lattice tool	FPGA chips
MicroBlaze	32-bit Xilinx core, free with tools, clones available	FPGA chips
NIOS II	32-bit Altera core, free with tools	FPGA chips
OpenRISC 1000	32-bit from people at Beyond Semiconductor who target ASICs with BA12-25 series	IP
PicoBlaze	8-bit Xilinx core, free with tools, clones available	FPGA chips
S8051XC3	highest performance 8051 clone, by CAST Inc., targets ASICs	IP
TSK3000A	32-bit RISC, Altium core, free with tools	CAD tools
ZPU	opensource.Zylin, "ZPU the worlds smallest 32 bit CPU with GCC toolchain"	design services

FPGA based Legacy Processor Emulation	http://en.wikipedia.org/wiki/Home_computer_remake
Sun Sparc	http://en.wikipedia.org/wiki/LEON
Cray-1 (cray1)	www.chrisfenton.com/homebrew-cray-1a/
PDP	http://www.aracnet.com/~healyzh/pdp_fpga.html
PDP-8	http://www.emeritus-solutions.com/pdp8onanfpga.htm
PDP-11/70 (w11)	http://opencores.org/project,w11
Amiga (68000)	http://en.wikipedia.org/wiki/Minimig
MIST(minimig)	http://harbaum.org/till/mist/index.shtml
SWTPC 6809	http://members.optusnet.com.au/jekent/system09/
Color Computer	http://8littlebits.wordpress.com/category/coco3fpga/
generic	http://fpgaarcade.com/

Other Insights

For small micro-controllers with small memory needs, some soft cores are competitive with ASIC cores

For a good figure of merit must keep LUT count low and fmax high

Floating-point will add at least 2K LUTs, except Altera now provides 32-bit floating-point in their series-10 DSP blocks

Both microBlaze and NIOS-2 have very good figure-of-merit numbers

If RAM area removed from ARM Cortex A9 ASIC, it has the highest figure of merit

There are "wrinkles" in CAD tools:

For ISE, Quartus and Vivado: success in inferring RAM and multipliers varies across vendor families & between vendors

For ISE, Quartus and Vivado: Fmax can vary in unpredicable ways across vendor families & between vendors

Two high performance ideas that work

Multi-threading or pipeline "barrel" increase performance without adding complexity: octavo, hive, or1200_hp

State machine with program as logic for programs under 200 instructions: iDEA, Lutiac, C-to-Hardware (HLS)

No one architecture dominates in performance, size or speed

Many clone and legacy designs have relatively poor figure of merit, usually due to high LUT counts

SoC designs usually have higher LUT counts, often 2X greater

For usable original designs the numbers are RISC is 47%, stack 20%, accumulator 15%, other 11%, OpenRisc 7%

Some opencores "alpha" phase designs are system designs where core is stable and working

For those barrel designs with adjustable barrel length, intermediate barrel length gives best KIPS/LUT (sample size of 2)

Only 28nm part families in webpack tools are Cyclone V, Atrix-7, Kintex-7 and Zynq-7

No parts from highest performance FPGA families available in "webpack" tools (Arria V, Stratix V, Virtex-7)

Designs with floating point

	cray1, fpgammix & s1_core are 64-bit, pdp2011 & oc54x 16-bit, others are 32-bit		LUT cnt	LUT type
ARM_Cortex_A9	ASIC, dual issue, includes fltg-pt & MMU & caches	std	4500	area equivalent
cray1	homebrew Cray1, double precision	std	13463	6LUT
fpgammix	clone of Knuth's MMIX, double precision	std	11605	ALUT

lemberg	upto 4 inst/clock	std	37459	4LUT
minsoc	minimal OR1200, vendor neutral, has caches	std	4945	6LUT
or1200_hp	1 to 4 slot barrel version of OR1200	std	5602	6LUT
pdp2011	clone of PDP11/34	std	5060	6LUT
risc5	minimalist Wirth, part of Project Oberon 2013	std	2441	6LUT
s1_core	reduced version of OpenSPARC T1	std	52845	6LUT
leon	SPARC, customized for ~50 FPGA boards, configurable	opt		
microblaze	Xilinx RISC, fltg-pt, cache & MMU options	opt		
nios2	Altera RISC, fltg-pt, cache & MMU options	opt		
Altera IP	variable exponent and mantissa size, sqrt , exp/log & trig avail, no denorm support	IP		
several	OpenCores Arithmetic cores	IP		
VHDL 2008	variable exponent and mantissa size, sqrt avail, denorms opt, rounding modes opt	IP		
Xilinx IP	variable exponent and mantissa size, sqrt & exp/log avail, no denorm support	IP		

Designs with ROM or RAM initialization	©2014 James Brakefield	
ROM/RAM inferred, MIF or other initialization		P&R on:
altor32	automatic use of either Altera LPMs or Xilinx primitives, no initialization	A&X
amber	generic_sram_byte_en.v: inferred byte enable RAM, also spartan-6 BRAM init	A&X
ao68000	MIF microcode file, see line 2130 of ao68000.v	A2
atlas_core	case statement in BOOT_MEM.vhd	X&A
c16	bit_vector constants in mem_conten.vhd, see memory.vhd: RAM4_S1_S1	S3
cray1	cray_rom.txt: xilinx MIF, see cray_sys_top.v line 111	K7
dalton_8051	constant in i8051_rom.vhd	K7
diogenes	MIF files , see pmem.vhd line 116	K7
eco32	large case based state "microcode" machine: cpu.v, no inferred RAM for Altera	X&A-
fpgammix	initmem.data: see progmem.v	A2
gumnut	source reads *.dat files, both VHDL & Verilog	A&X
gup	gucode.mif: see gucode.vhd line 89	A2
hd63701	*.i include files contain table definitions: see HD63701_MCROM.v	S3&6
lem1_9min	lem1_9min.vhd has array constant, for Quartus to infer block RAM, must be fully registered	X&A
leros	leros_rom.vhd: case statement with others	X&A
light52	light52_ucode_pkg.vhd has microcode table generator	C2&X
light8080	light808.vhdl has signal array init (instead of constant init)	X&A-
lwrisc	init_file.mif: see ramxxx.v files	A2
m1_core	*.vh initialization file	X&A
m16c5x, p16c5x	COE files	X&A
marca	Altera memory IP & MIF files	A2
natalius_8bit_risc	inferred, MEM file	X
nige_machine	MIF files	K7
pdp8l	MIF files	C3
plasma	INIT text	K7
risc0	INIT text	K7
risc5	MEM file	X&A
rtf68ksys	case statement in bootrom.v	S3
system68	INIT in xilinx RAMB4_S8	S3
t51	case table	K7&A2
z80soc	COE files	S3&C3