LPC Bridge Core Specification

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Revision History

Rev.	Date	Author	Description
0.1	03/01/2008	Howard M. Harte	First Draft
02.	03/05/2008	Howard M. Harte	Corrected some mistakes.

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Introduction

The
The core features an 32-bit wishbone interface.

FEATURES:

- Compliant to Intel(r) Low Pin Count (LPC) Interface Specification Revision 1.1
- Wishbone Slave to LPC Host Module
  - Memory Read and Write (1-byte)
  - I/O Read and Write (1-byte)
  - Firmware Memory Read and Write (1-, 2- and 4-byte)
- Wishbone Master to LPC Peripheral Module
  - Memory Read and Write (1-byte)
  - I/O Read and Write (1-byte)
  - Firmware Memory Read and Write (1-, 2- and 4-byte)
- Fully static synchronous design with one clock domain
- Technology independent Verilog
- Fully synthesizable

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LPC Host IO ports

2.1 WISHBONE Slave to LPC Host Interface Connections

Port	Width	Direction	Description
clk_i	1	Input	Master clock input
nrst_i	1	Input	Asynchronous active low reset
wbs_inta_o	1	Output	Interrupt request signal
wbs_cyc_i	1	Input	Valid bus cycle
wbs_stb_i	1	Input	Strobe/Core select
wbs_adr_i	2	Input	Lower address bus bits
wbs_tga_i	2	Input	
wbs_sel_i	4	Input	
wbs_we_i	1	Input	Write enable
wbs_dat_i	8	Input	Data input
wbs_dat_o	8	Output	Data output
wbs_ack_o	1	Output	Normal bus termination

2.1.1 clk_i
All internal WISHBONE logic is registered to the rising edge of the [clk_i] clock input.

2.1.2 rst_i
The active low asynchronous reset input [rst_i] forces the core to restart. All internal registers are preset and all state-machines are set to an initial state.

2.1.3 wbs_inta_o
The interrupt request output is asserted when the core needs service from the host system.

2.1.4 wbs_cyc_i
When asserted, the cycle input [cyc_i] indicates that a valid bus cycle is in progress. The logical AND function of [cyc_i] and [stb_i] indicates a valid transfer cycle to/from the core.

2.1.5 wbs_stb_i
The strobe input [stb_i] is asserted when the core is being addressed. The core only responds to WISHBONE cycles when [stb_i] is asserted, except for the [rst_i], which always receive a response.

2.1.6 wbs_adr_i

The address array input [adr_i] is used to pass a binary coded address to the core. The most significant bit is at the higher number of the array.

2.1.7 wbs_tga_i
The address tag input, defines transfer type on LPC Bus (I/O, Memory, DMA, Firmware.

WB_TGA_MEM	Memory Cycle	2'b00
WB_TGA_IO	I/O Cycle	2'b01
WB_TGA_FW	Firmware Memory Cycle	2'b10
WB_TGA_DMA	DMA Cycle	2'b11

2.1.8 wbs_sel_i
Select lines that determine the access size and byte lanes on the Wishbone backplane.

2.1.9 wbs_we_i
When asserted, the write enable input [we_i] indicates that the current bus cycle is a write cycle. When negated, it indicates that the current bus cycle is a read cycle.

2.1.10 wbs_dat_i
The data array input [dat_i] is used to pass binary data from the current WISHBONE Master to the core. All data transfers are 8 bit wide.

2.1.11 wbs_dat_o
The data array output [dat_o] is used to pass binary data from the core to the current WISHBONE Master. All data transfers are 8 bit wide.

2.1.12 wbs_ack_o
When asserted, the acknowledge output [ack_o] indicates the normal termination of a valid bus cycle.

2.2 External (LPC Host Port) Connections

Port	Width	Direction	Description
lpc_clk_o	1	Output	LPC clock
lframe_o	1	Output	LPC LFRAME Signal
lad_o	4	Output	LPC Address/Data Bus Out
lad_i	4	Input	LPC Address/Data Bus In
lad_oe	1	Output	LPC Address/Data Output Enable

2.2.1 lpc_clk_o
Lpc_clk_o is generated by the master device and synchronizes data movement on the LPC Bus.

2.2.2 lframe_o
Frame: Indicates start of a new cycle, termination of broken cycle.

2.2.3 lad_o
The multiplexed LPC Command, Address, and Data Bus output.

2.2.4 lad_i
The multiplexed LPC Command, Address, and Data Bus input.

2.2.5 lad_oe
The multiplexed LPC Command, Address, and Data Bus output enable.

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LPC Peripheral IO ports

3.1 WISHBONE Master to LPC Peripheral Interface Connections

Port	Width	Direction	Description
clk_i	1	Input	Master clock input
rst_i	1	Input	Asynchronous active low reset
wbm_inta_i	1	Input	Interrupt request signal
wbm_cyc_o	1	Output	Valid bus cycle
wbm_stb_o	1	Output	Strobe/Core select
wbm_adr_o	2	Output	Lower address bus bits
wbm_tga_o	2	Output	
wbm_sel_o	4	Output	
wbm_we_o	1	Output	Write enable
wbm_dat_i	8	Input	Data input
wbm_dat_o	8	Output	Data output
wbm_ack_i	1	Input	Normal bus termination

3.1.1 clk_i
All internal WISHBONE logic is registered to the rising edge of the [clk_i] clock input.

3.1.2 rst_i
The active low asynchronous reset input [rst_i] forces the core to restart. All internal registers are preset and all state-machines are set to an initial state.

3.1.3 inta_i
The interrupt request output is asserted when the core needs service from the host system.

3.1.4 cyc_o
When asserted, the cycle input [cyc_i] indicates that a valid bus cycle is in progress. The logical AND function of [cyc_i] and [stb_i] indicates a valid transfer cycle to/from the core.

3.1.5 stb_o
The strobe input [stb_i] is asserted when the core is being addressed. The core only responds to WISHBONE cycles when [stb_i] is asserted, except for the [rst_i], which always receive a response.

3.1.6 adr_o

The address array input [adr_i] is used to pass a binary coded address to the core. The most significant bit is at the higher number of the array.

3.1.7 wbm_tga_o
The address tag output, indicates transfer type on LPC Bus (I/O, Memory, DMA, Firmware.

WB_TGA_MEM	Memory Cycle	2'b00
WB_TGA_IO	I/O Cycle	2'b01
WB_TGA_FW	Firmware Memory Cycle	2'b10
WB_TGA_DMA	DMA Cycle	2'b11

3.1.8 wbm_sel_o
Select lines that determine the access size and byte lanes on the Wishbone backplane.

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When asserted, the write enable input [we_i] indicates that the current bus cycle is a write cycle. When negated, it indicates that the current bus cycle is a read cycle.

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The data array input [dat_i] is used to pass binary data from the current WISHBONE Master to the core. All data transfers are 8 bit wide.

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The data array output [dat_o] is used to pass binary data from the core to the current WISHBONE Master. All data transfers are 8 bit wide.

3.1.12 wbm_ack_i
When asserted, the acknowledge output [ack_o] indicates the normal termination of a valid bus cycle.

3.2 External (LPC Peripheral Port) Connections

Port	Width	Direction	Description
lpc_clk_i	1	Input	LPC Clock
lframe_i	1	Input	LPC LFRAME Signal
lad_o	4	Output	LPC Address/Data Bus Out
lad_i	4	Input	LPC Address/Data Bus In
lad_oe	1	Output	LPC Address/Data Output Enable

3.2.1 lpc_clk_i
Lpc_clk_o is generated by the master device and synchronizes data movement on the LPC Bus.

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Frame: Indicates start of a new cycle, termination of broken cycle.

3.2.3 lad_o
The multiplexed LPC Command, Address, and Data Bus output.

3.2.4 lad_i
The multiplexed LPC Command, Address, and Data Bus input.

3.2.5 lad_oe
The multiplexed LPC Command, Address, and Data Bus output enable.

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Operation

4.1 LPC Transfers

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