



Gisselquist
Technology, LLC

The ZipCPU

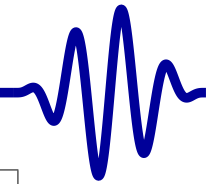
A resource efficient
32-bit SoftCore CPU

Daniel E. Gisselquist, Ph.D.
October, 2016





Survey of CPUs



Feature	Nios	μ Blaze	ECO-32	RISC-V	OpenRISC	ZipCPU
Open Architecture?	No		Yes			
Number of Instructions	86	129	61	50	219	
OpCode Bits	6-17	6-11	6	10	6-32	
Interrupt/Exception Vectors	1	6	2	9+	14	
Register Indirect plus displacement (bits)	16	16	16	12	16	
Immediate direct addressing (bits)	16, using R0=0					
Relative branching (bits)	16		26 (28)	21	26	
Conditional branching (bits)	16		16 (18)	13	26	
Register Size (bits)	32			32(64)		
Special Purpose Registers	6	25	6	66+	65+	
General Purpose Registers	32 (but R0=0, others are unusable, ... 24)					
8-bit data	Yes					
16-bit data	Yes					
32-bit data	Yes					
64-bit data	No	No	Emul	Yes, by extension		
32-bit floats	Optional		No	Yes, by extension		
64-bit floats	No	No	No	Yes, by Extension		
Vector instructions	No	No	No	Not yet	64-bits, Ext	
MMU	Yes, but optional					
Instruction Cache	Yes, configurable					
Data Cache	Yes, configurable					