

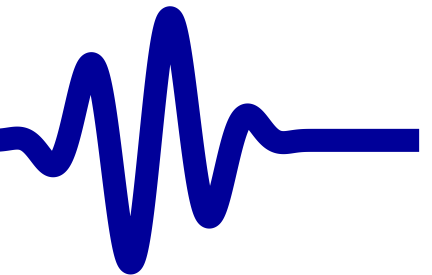


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The ZipCPU

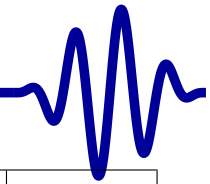
A resource efficient
32-bit SoftCore CPU

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Survey of CPUs



Feature	NiOS	μ Blaze	ECO-32	RISC-V	OpenRISC	LM32	ZipCPU
Open Architecture?	No		Yes				
Number of Instructions	86	129	61	50+	48+	62	
OpCode Bits	6-17	6-11	6	10	6-32	6	
Interrupt/Exception Vectors	1	6	2	9+	14	32	
Register Indirect plus displacement (bits)	16			12	16		
Immediate direct addressing (bits)	16, using R0=0						
Relative branching (bits)	16		26 (28)	21	26	21	
Conditional branching (bits)	16		16 (18)	13	26	16	
Register Size (bits)	32			32 (Opt. 64 Exts.)		32	
Special Purpose Registers	6	25	6	66+	65+	10	
General Purpose Registers	32 (but R0=0, others are unusable, ... 24)						
8-bit data	Yes						
16-bit data	Yes						
32-bit data	Yes						
64-bit data	No			Yes, by extension		No	
32-bit floats	Optional		No	Yes, by extension		No	
64-bit floats	No			Yes, by extension		No	
Vector instructions	No			Not yet	64-bits, Ext	No	
MMU	Yes, but optional						
Instruction Cache	Yes, configurable						
Data Cache	Yes, configurable						

To be revealed at ORCONF 2016